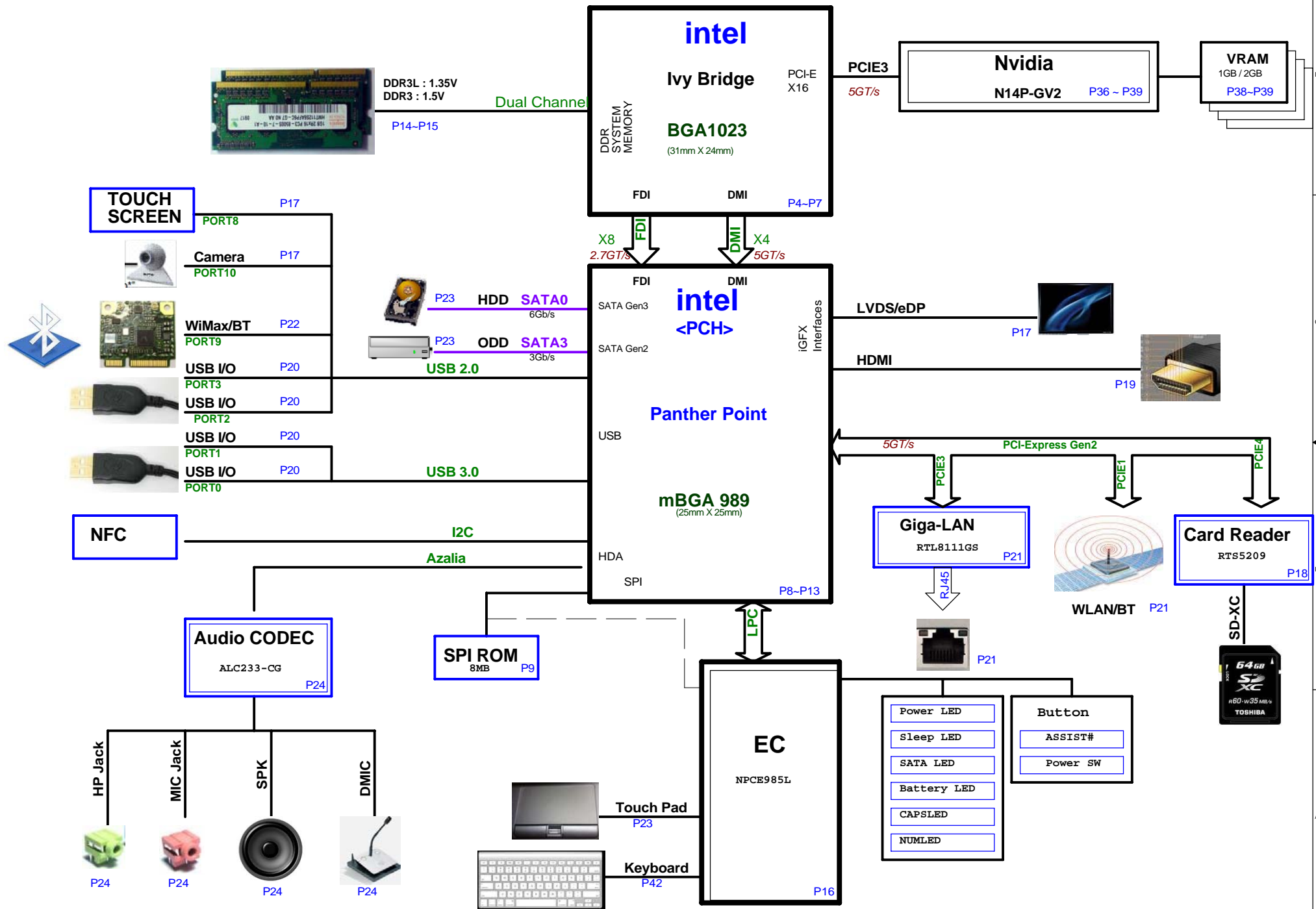


</

# Chief River ULV BLOCK DIAGRAM

02



**Change List**

**MB\_SCH\_PVT\_001**

P22-Add R333 0\_6S.

P22- U15 don't mount

P22-Add Q32(2N7002).

P22-Add R335(100K\_4).

Reason : Modify circuit for KB Backlight.

Possible Risk: No.

**MB\_SCH\_PVT\_002**

P23-CON11.11 delete net"DATA\_ODD\_DA#

P10-U17.G40 delete net"SATA\_ODD\_DA#".

P10-Delete R64(10K\_4).

Reason : Modify circuit for Zero Power ODD.

Possible Risk: No.

**MB\_SCH\_PVT\_002**

P08-ADD 0.1UF on "PCH\_PWROK\_EC"

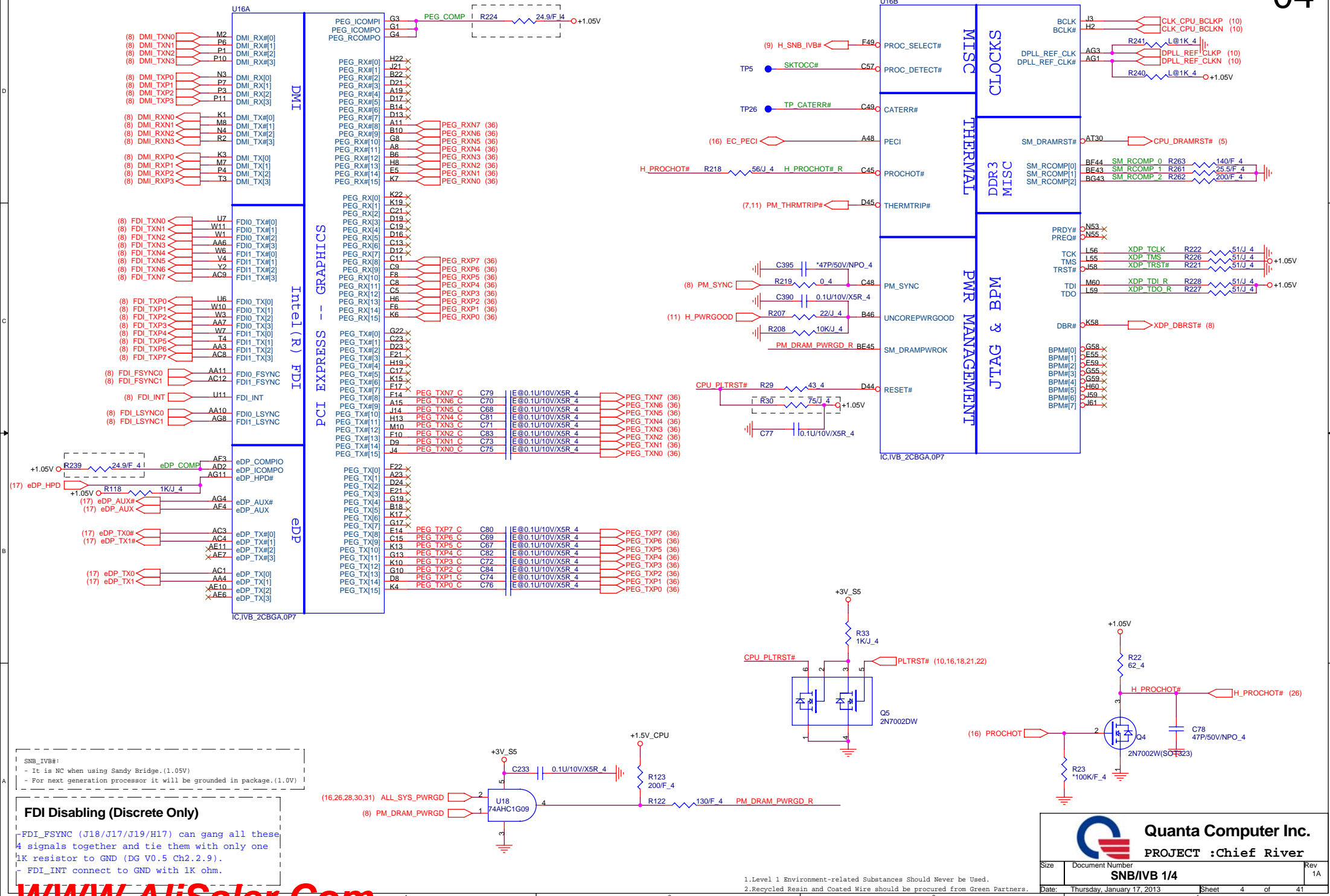
Reason : Modify circuit for ESD.

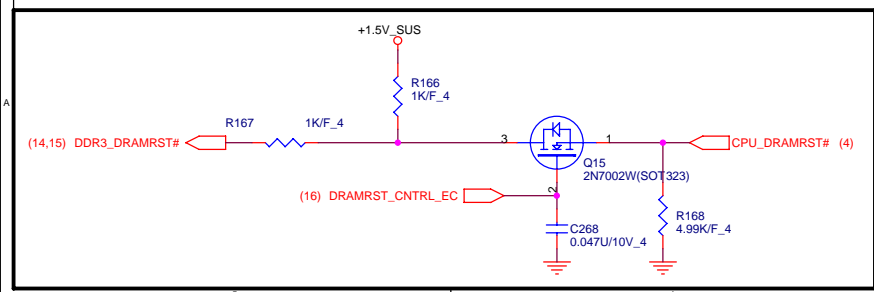
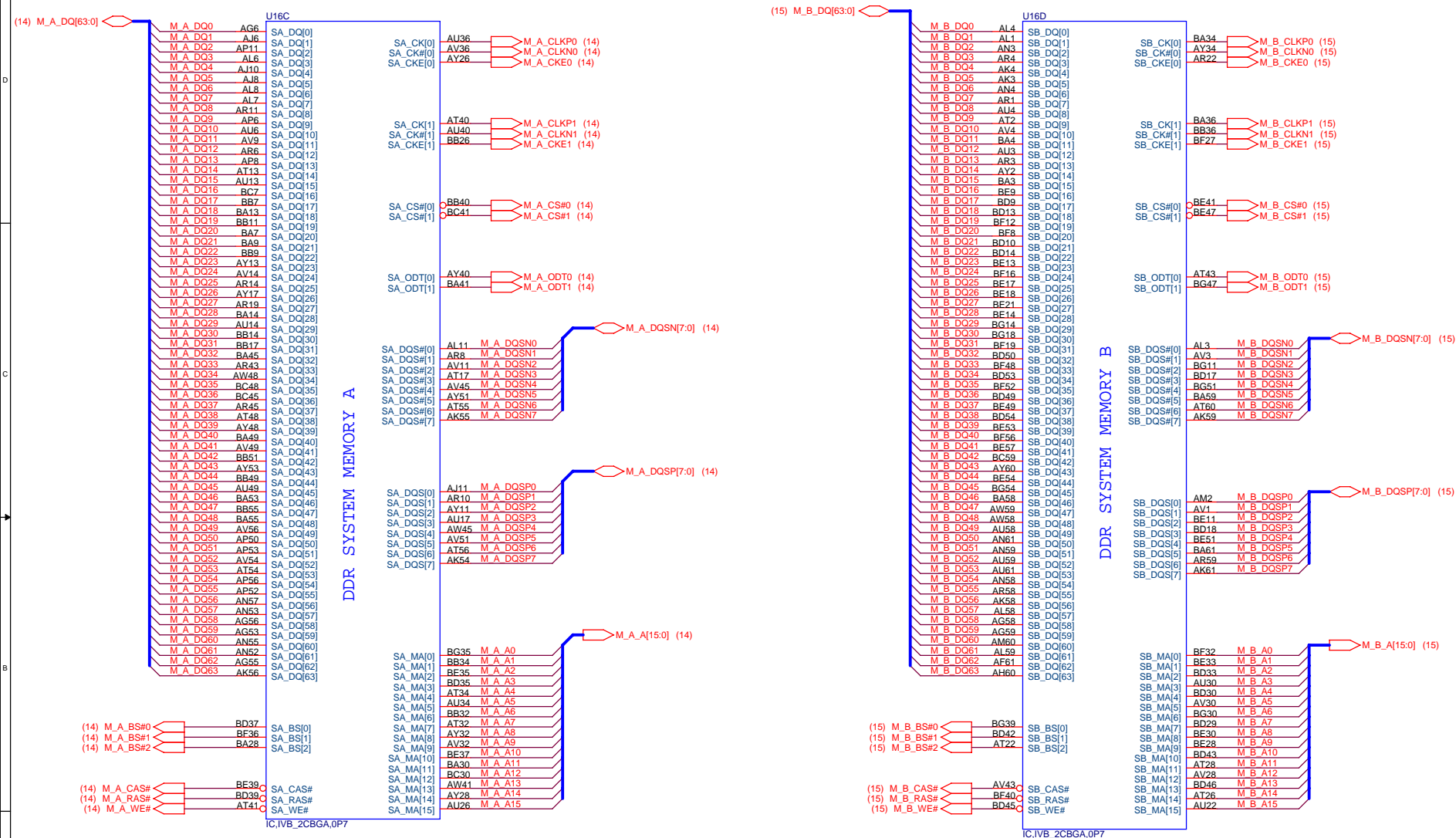
Possible Risk: No.

## Ivy Bridge Processor (DMI,PEG,FDI)

## Ivy Bridge Processor (CLK,MISC,JTAG)

04





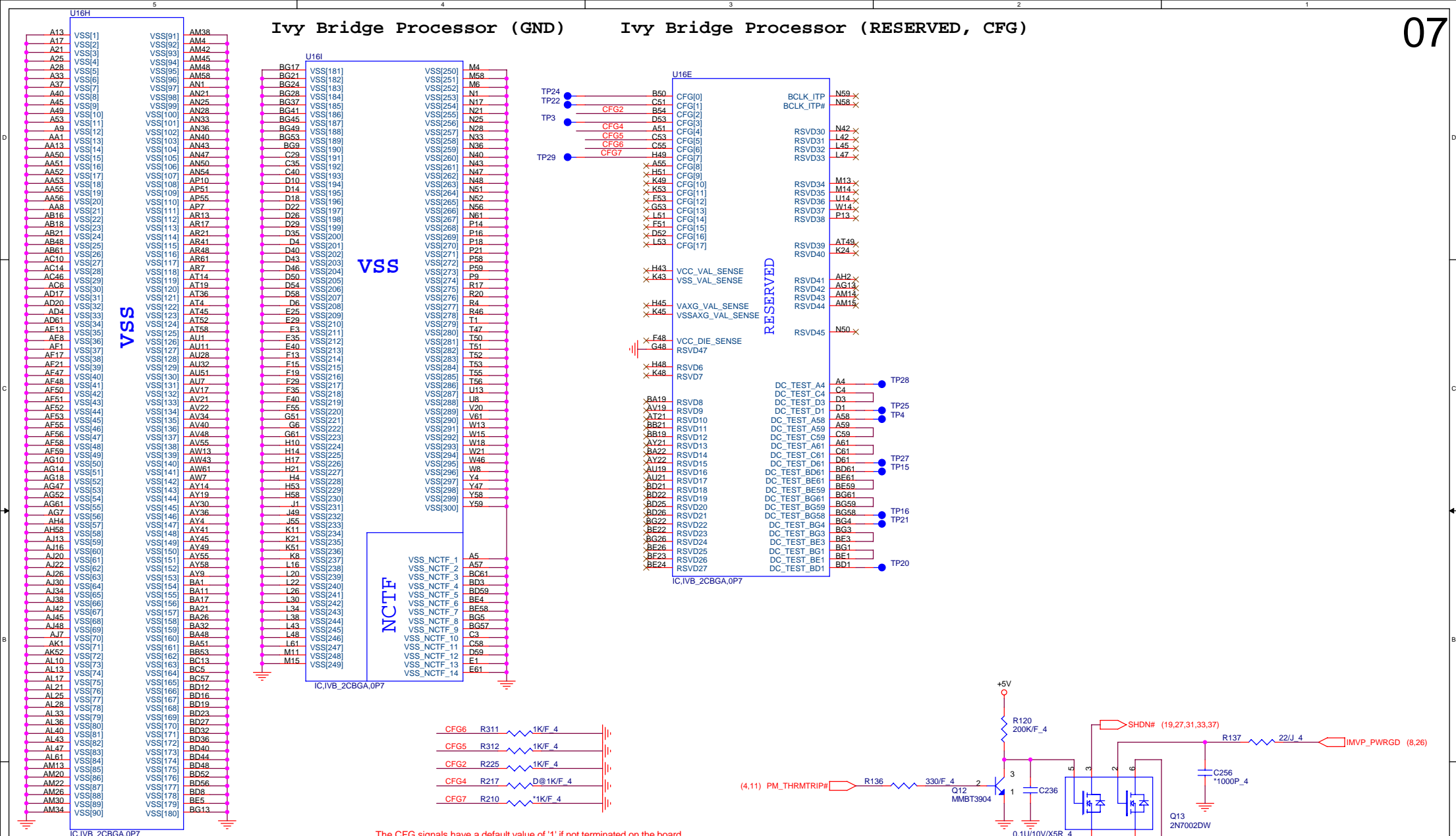
Quanta Computer Inc.  
PROJECT :Chief River

Size: Document Number: SNB/IVB 2/4 Rev 1A

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Thursday, January 17, 2013 Sheet 5 of 41



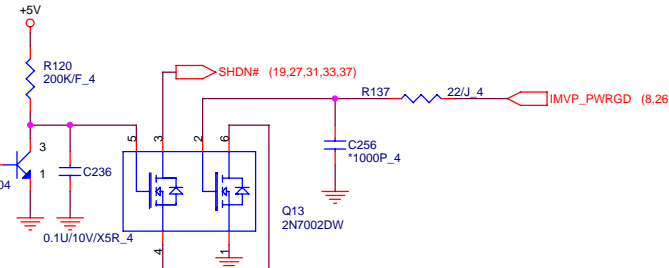


## Processor Strapping

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	<b>Disable; No physical DP attached to eDP</b>	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	<b>PEG train immediately following xxRESETB de assertion</b>	PEG wait for BIOS training

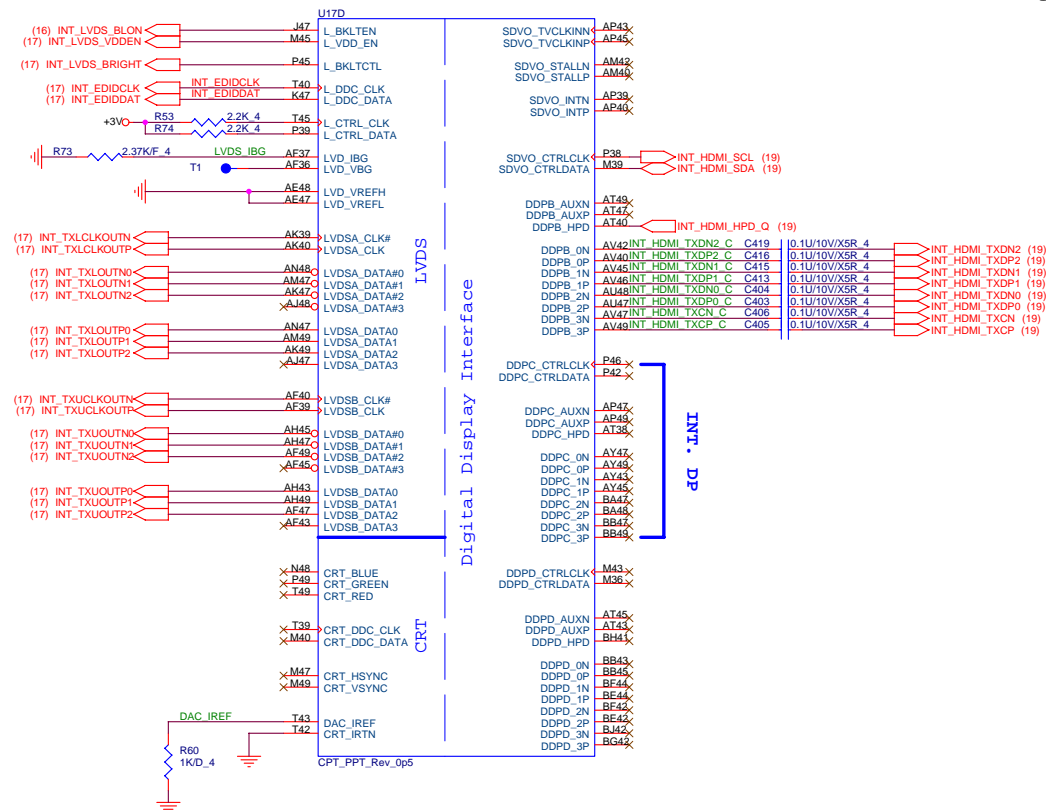
### CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enableddisabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```





CPT/PPT (LVDS,DDI)



**PCB Pull-up/down (CLG)**

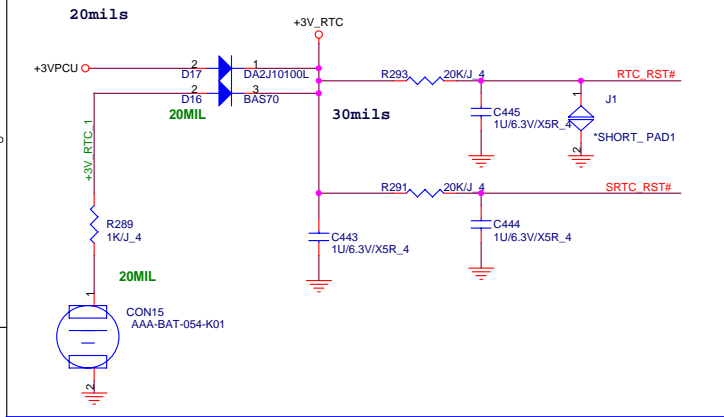
The schematic diagram illustrates the pull-up and pull-down configurations for various signals on the PCB. The components and their connections are as follows:

- CLKRUN#**: Connected to **+3V** through resistor **R148** (8.2K/J 4).
- XDP\_DBRST#**: Connected to **+3V** through resistor **R278** (1K/J 4).
- PWROK\_R**: Connected to **GROUND** through resistor **R169** (47K 4).
- PM\_RI#**: Connected to **+3V\_S5** through resistor **R267** (10K/J 4).
- SUSWARN#**: Connected to **+3V\_S5** through resistor **R108** (10K/J 4).
- PM\_BATLOW#**: Connected to **+3V\_S5** through resistor **R135** (8.2K/J 4).
- AC\_PRESENT**: Connected to **+3V\_S5\_DSW** through resistor **R105** (\*10K/J 4).
- PM\_DRAM\_PWRGD**: Connected to **+3V\_SUS** through resistor **R265** (200/F 4).
- PCIE\_WAKE#**: Connected to **+3V\_S5** through resistor **R269** (10K/J 4).
- +3V\_RTC**: Connected to **DSWVREN** through resistor **R254** (330K/J 4).

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

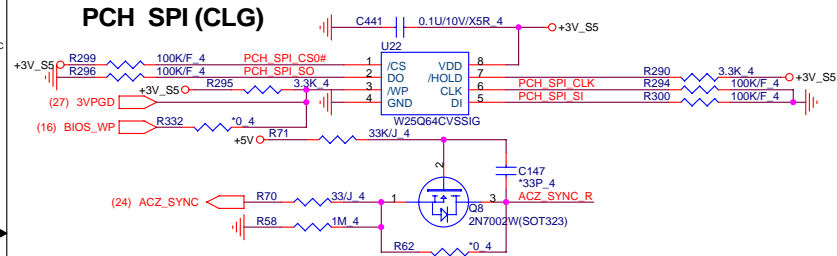


## RTC Circuitry(RTC)



MX25L3205DM2I-12G: AKE39FP0Z00  
W25X32VSSIG: AKE39ZP0N00

## PCH SPI (CLG)



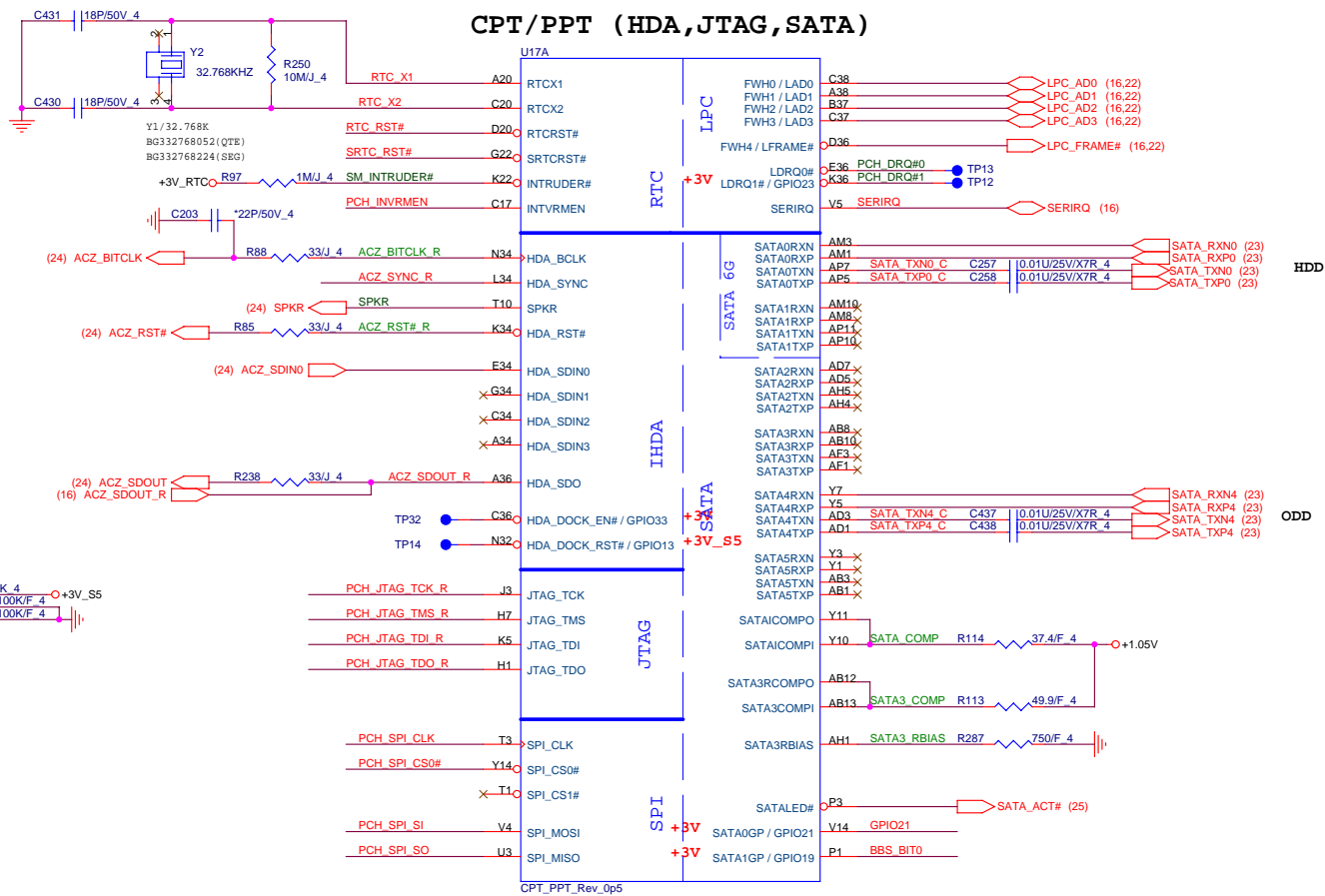
(16) F\_CS0#\_PCH R298 0 4 PCH SPI CS0#  
(16) F\_SDI\_PCH R297 0 4 PCH SPI SO  
(16) SCK\_PCH R292 0 4 PCH SPI CLK  
(16) SD0\_PCH R301 0 4 PCH SPI SI

For NPCE885L Using

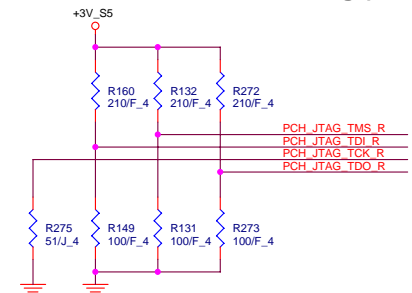
## PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR
PCI_GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	TP7  PCL_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R255 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	TP30  BBS_BIT1 (10) TP33  BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	ACZ_SDOOUT_R R282 2.2K 4 +1.8V R276 1K/J_4  NV_CLE (11) H_SNB_IVB# (4)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss for Ivy Bridge 1 = Set to Vcc for Sandy Bridge (weak pull-down 20K)	TP19  PLL_ODVR_EN (11)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R65 1K/J_4 ACZ_SYNC_R
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	

## CPT/PPT (HDA,JTAG,SATA)



## PCH JTAG Debug (CLG)



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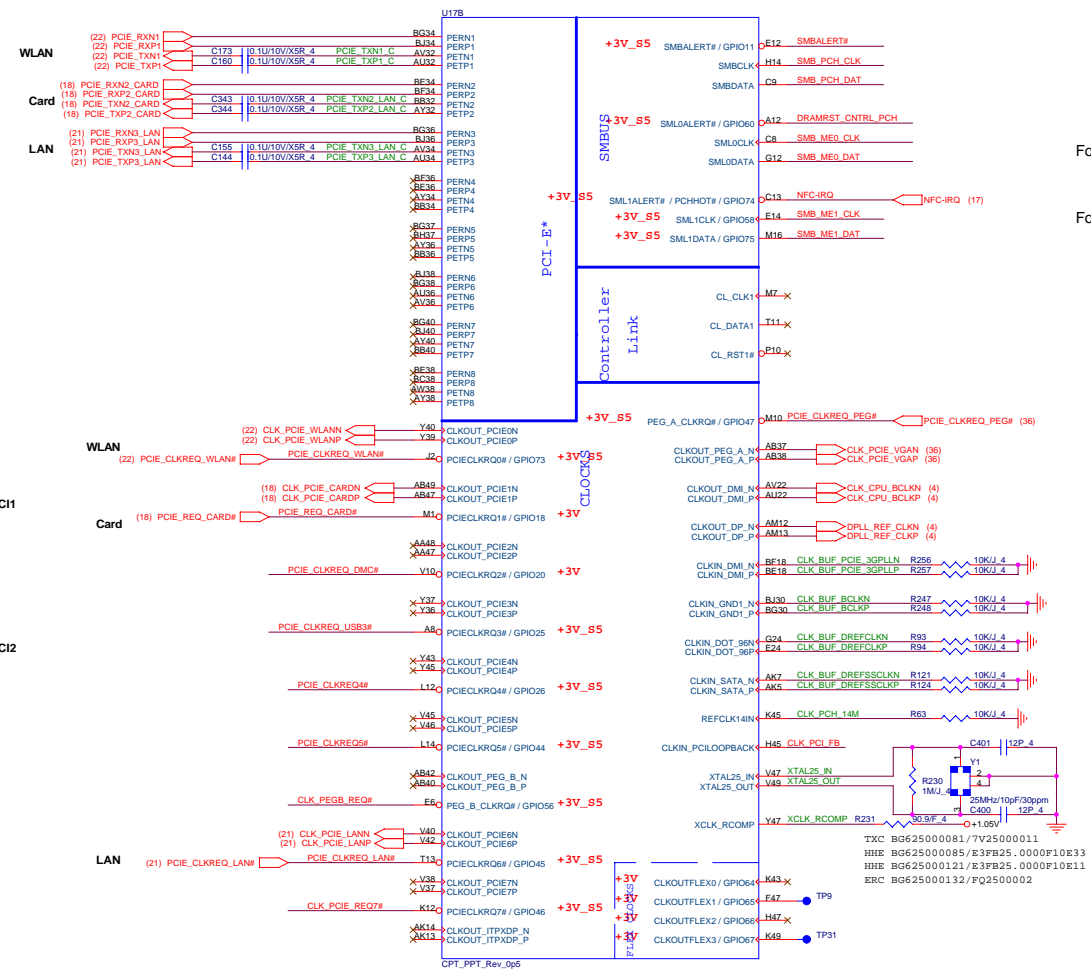
Size Document Number  
**CPT/PPT 2/6**

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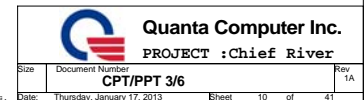
1.Level 1 Environment-related Substances Should Never be Used.

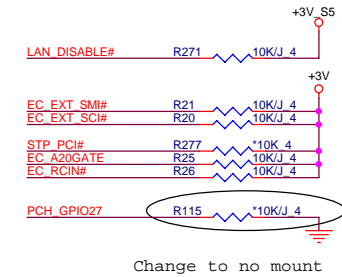
2.Recycled Resin and Coated Wire should be procured from Green Partners.

CPT/PPT (PCI-E, SMBUS, CLK)




For EC



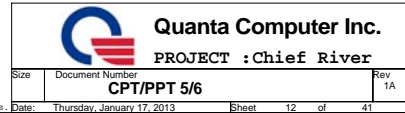


Pinout diagram for the 16-pin JST connector. The diagram shows two rows of pins. The top row (pins 1-8) has labels: R285 (10K/J 4), BOARD ID0, R286 (\*10K/J 4), and \*10K/J 4. The bottom row (pins 9-16) has labels: R82 (10K/J 4), BOARD ID1, R78 (10K/J 4), R56 (10K/J 4), BOARD ID2, R51 (10K/J 4), R151 (10K/J 4), BOARD ID3, R150 (10K/J 4), R145 (10K/J 4), BOARD ID4, and R155 (10K/J 4). A +3V supply is indicated at the top right.

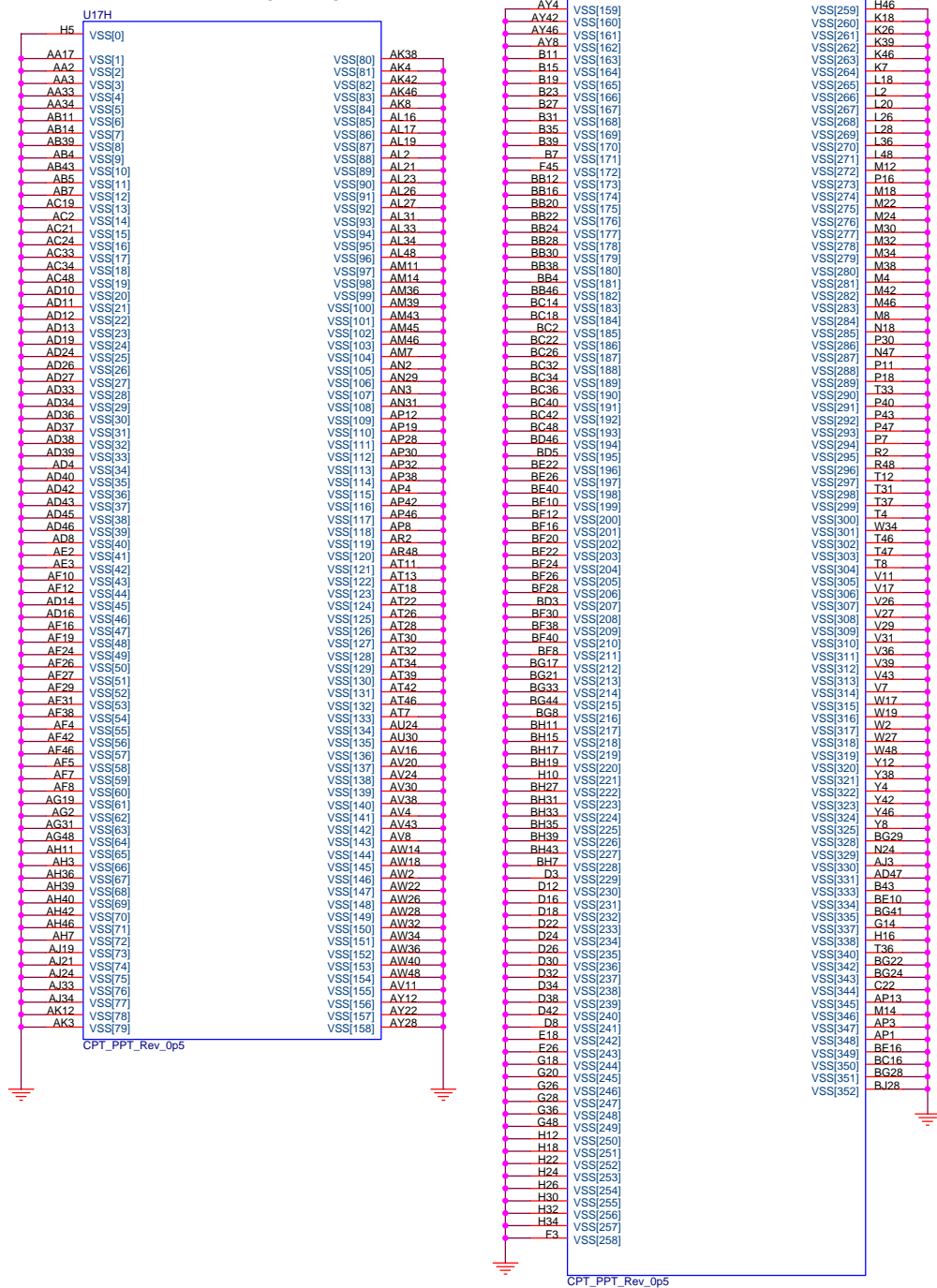
PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff

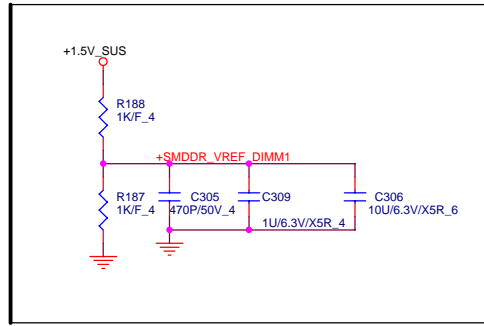
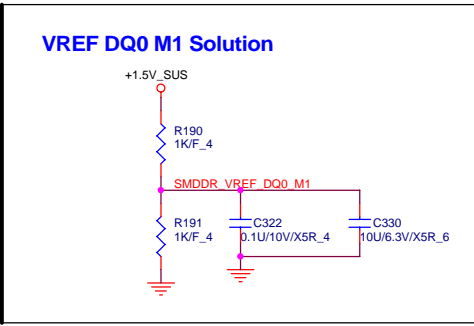
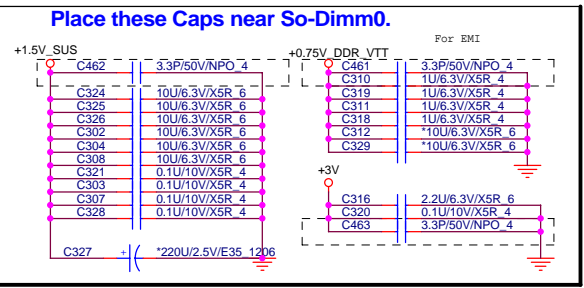
 **Quanta Computer Inc.**  
PROJECT :Chief River

- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners

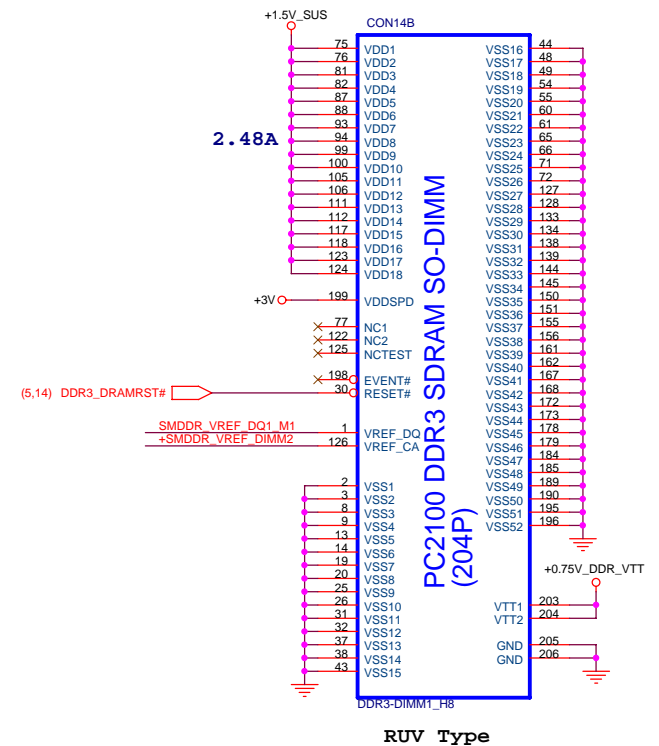


CPT/PPT (GND)

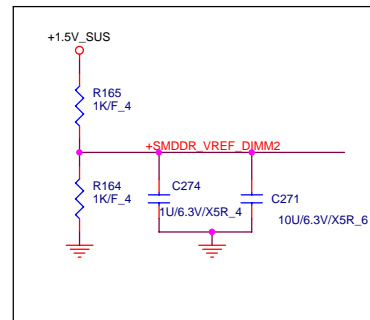






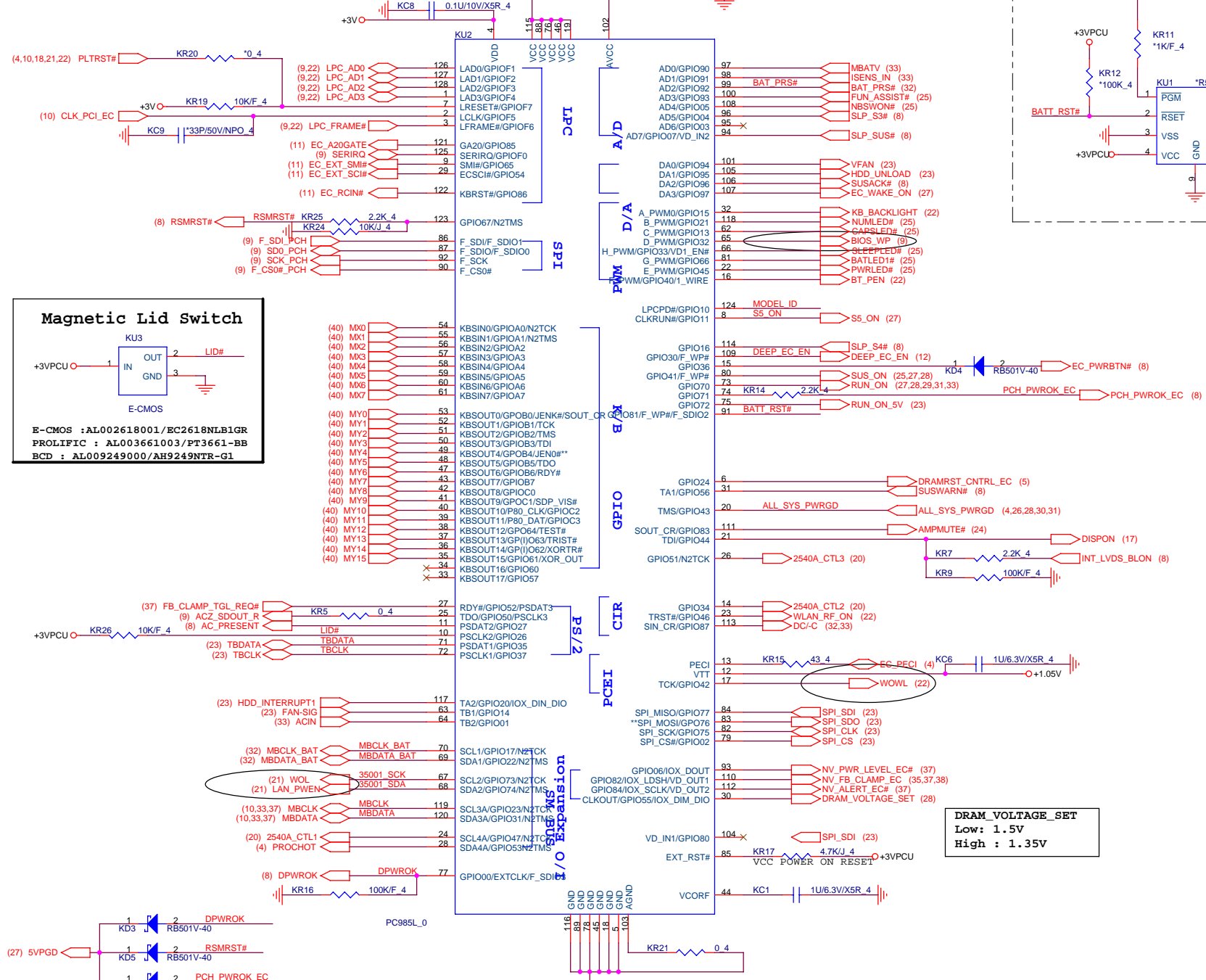


RUV Type



**\*\* Strapping Pin, Can not pull low.**  
Note the input leakage current to the strap pins must be less than 10uA.

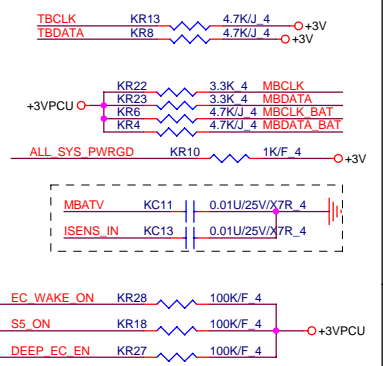
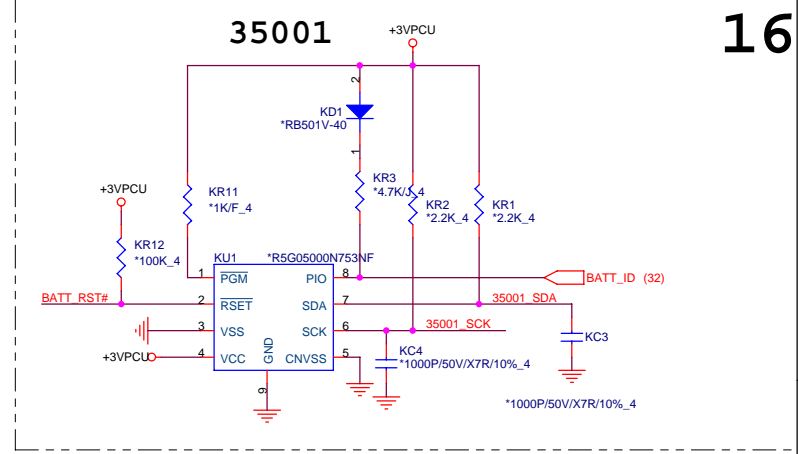
Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



**Magnetic Lid Switch**

Diagram of a magnetic lid switch circuit using an E-CMOS component (KU3). The circuit includes a 3VPCU supply, an IN pin, an OUT pin, and a LID# signal line. The GND pin is connected to ground.

E-CMOS : AL002618001/EC2618NLB1GR  
PROLIFIC : AL003661003/PT3661-BB  
BCD : AL009249000/AH9249NTR-G1

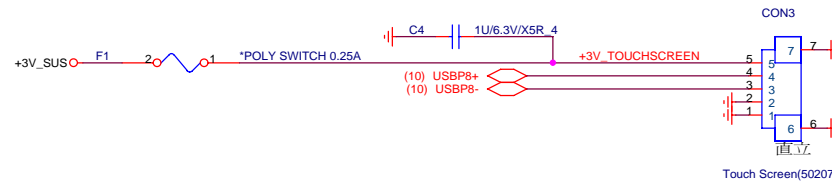


**DRAM VOLTAGE SET**  
Low: 1.5V  
High: 1.35V

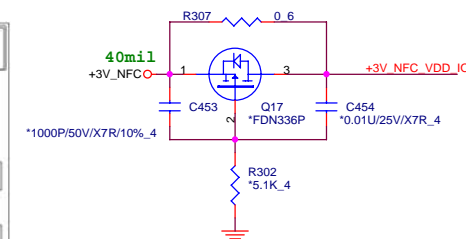
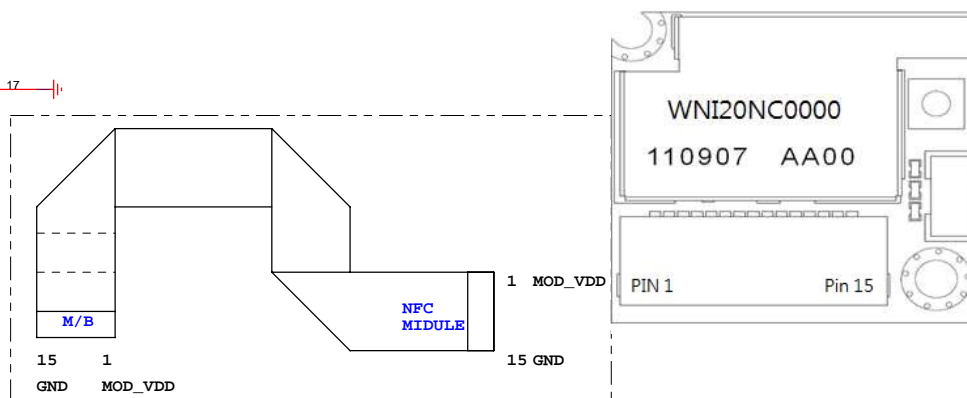
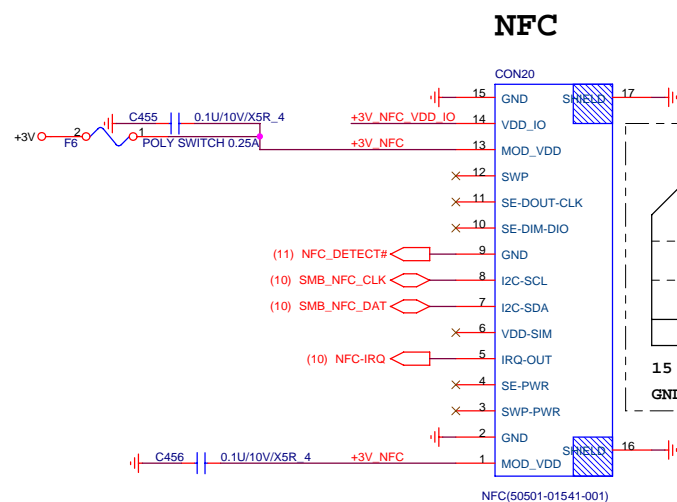
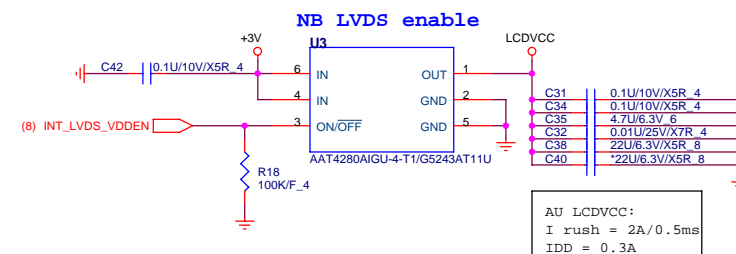
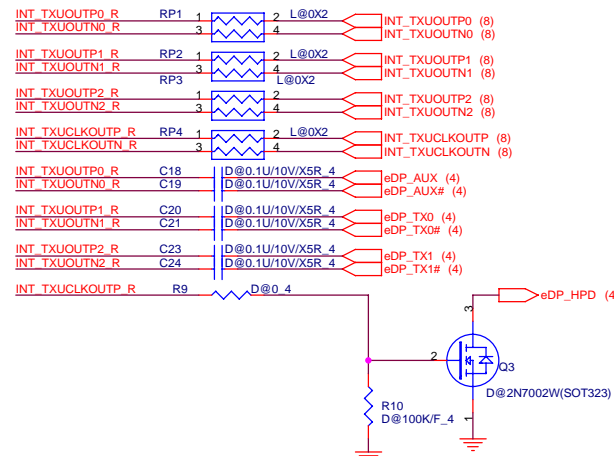
MODEL ID	
High	HK8/HK9(KR29 mount KR30 no mount)
Low	GD5/GD6(KR29 no mount KR30 mount)

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PROJECT :Chief River

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	NPC885L	1A
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NFC module :  
Vender : Samsung SNC-i20  
Power consumption : Max. 160mW/48mA  
Power Ripple +/- 50mV

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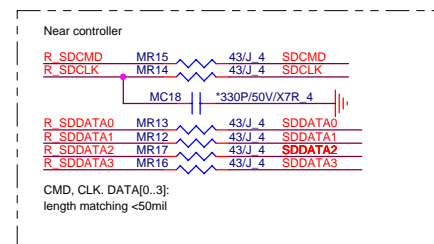
PROJECT :Chief River

**CRT/LVDS**

Rev  
1A

- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners

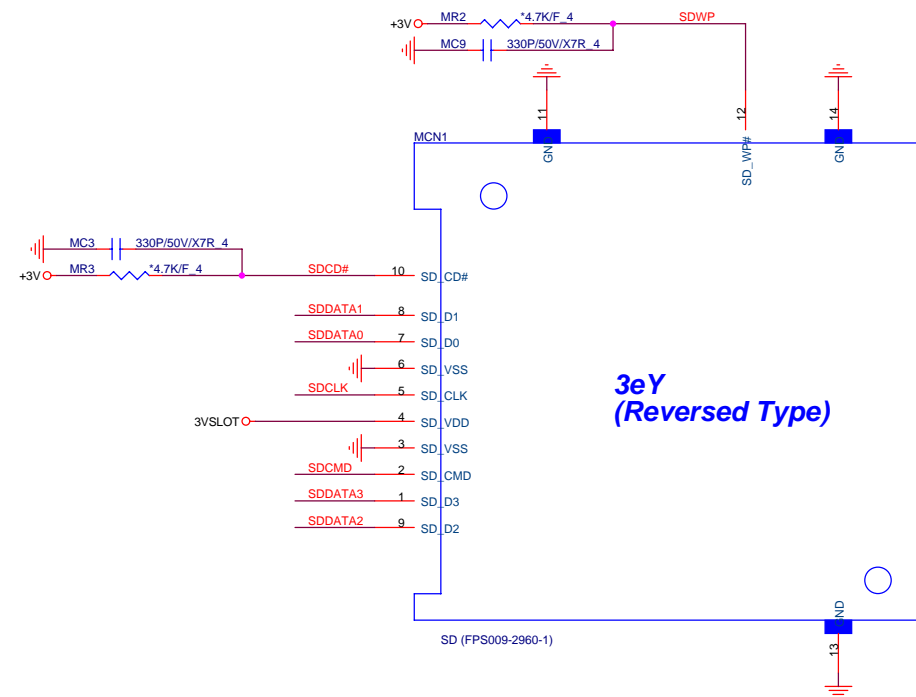
Date: Thursday, January 17, 2013 Sheet 17 of 41

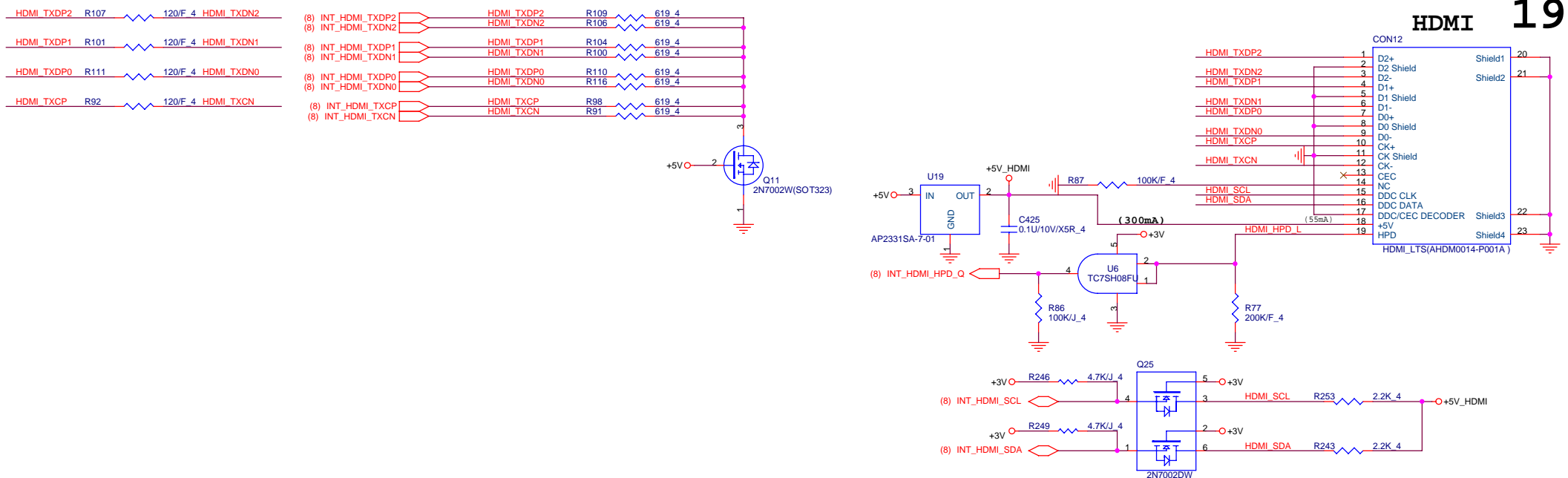


40 mil

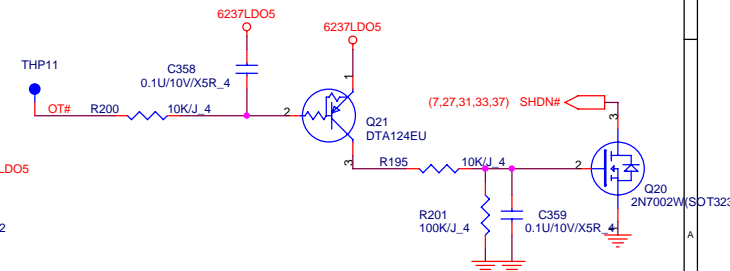
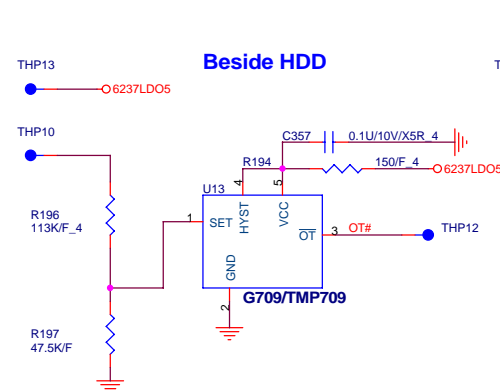
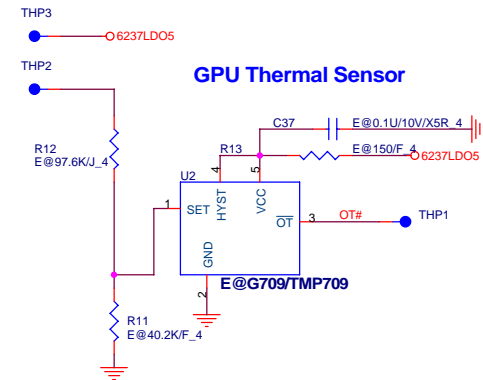
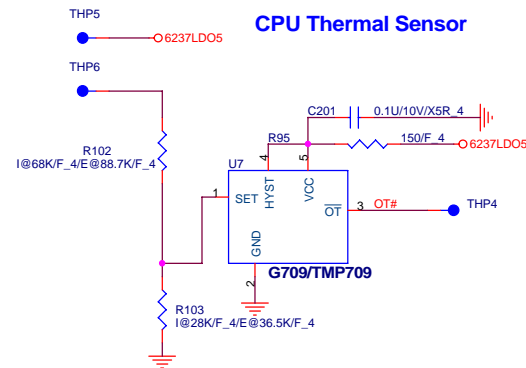
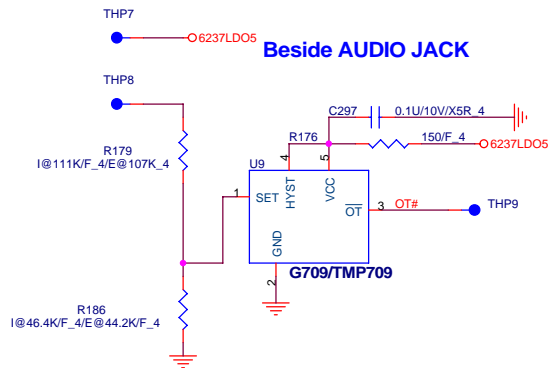
MC7 0.1U/10V/X5R\_4  
MC4 1U/6.3V/X5R\_4  
MC6 1U/6.3V/X5R\_4

3VSL0T





## H/W Thermal Protect



$$RSET(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

95	18.5K
100	15K
107	10.3K
110	8.2K

### DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	70	R208=36.87K	36.5K	71	70
Near GFX sensor temp	65	R146=40.72K	40.2K	66.3	65.1
Near AUDIO sensor temp	60	R345=44.62K	44.2K	61.2	60

### UMA SKU

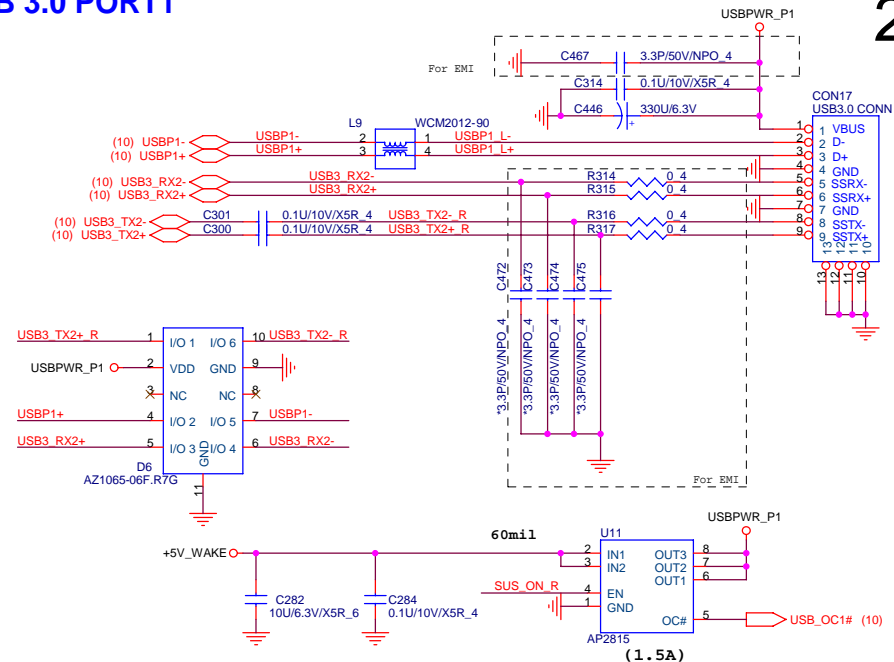
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	81	R208=28.63K	28K	82.3	81.4
Near AUDIO sensor temp	58	R345=46.2K	46.4K	58.4	57.1



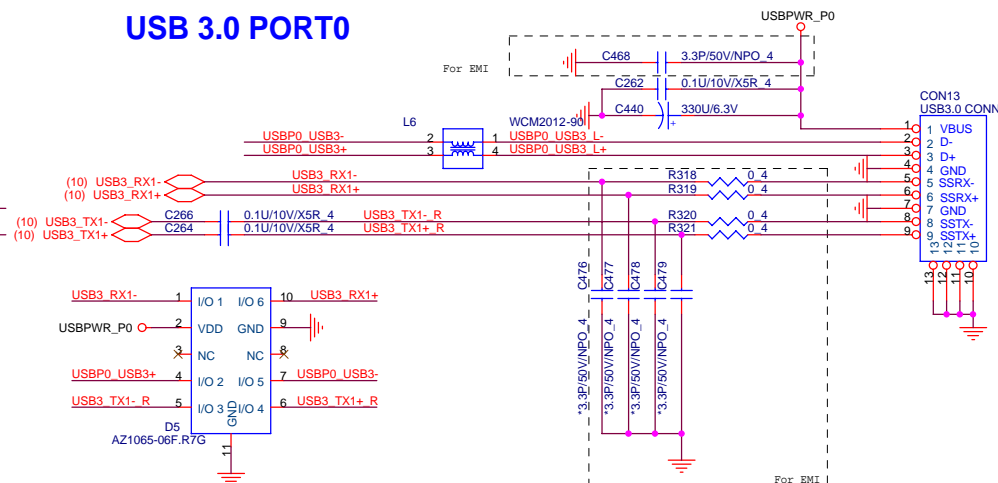
**Quanta Computer Inc.**  
PROJECT :Chief River

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<b>HDMI/Thermal IC</b>									

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.



## USB 3.0 PORT0




Mode CDP OFF DCP

VBUS

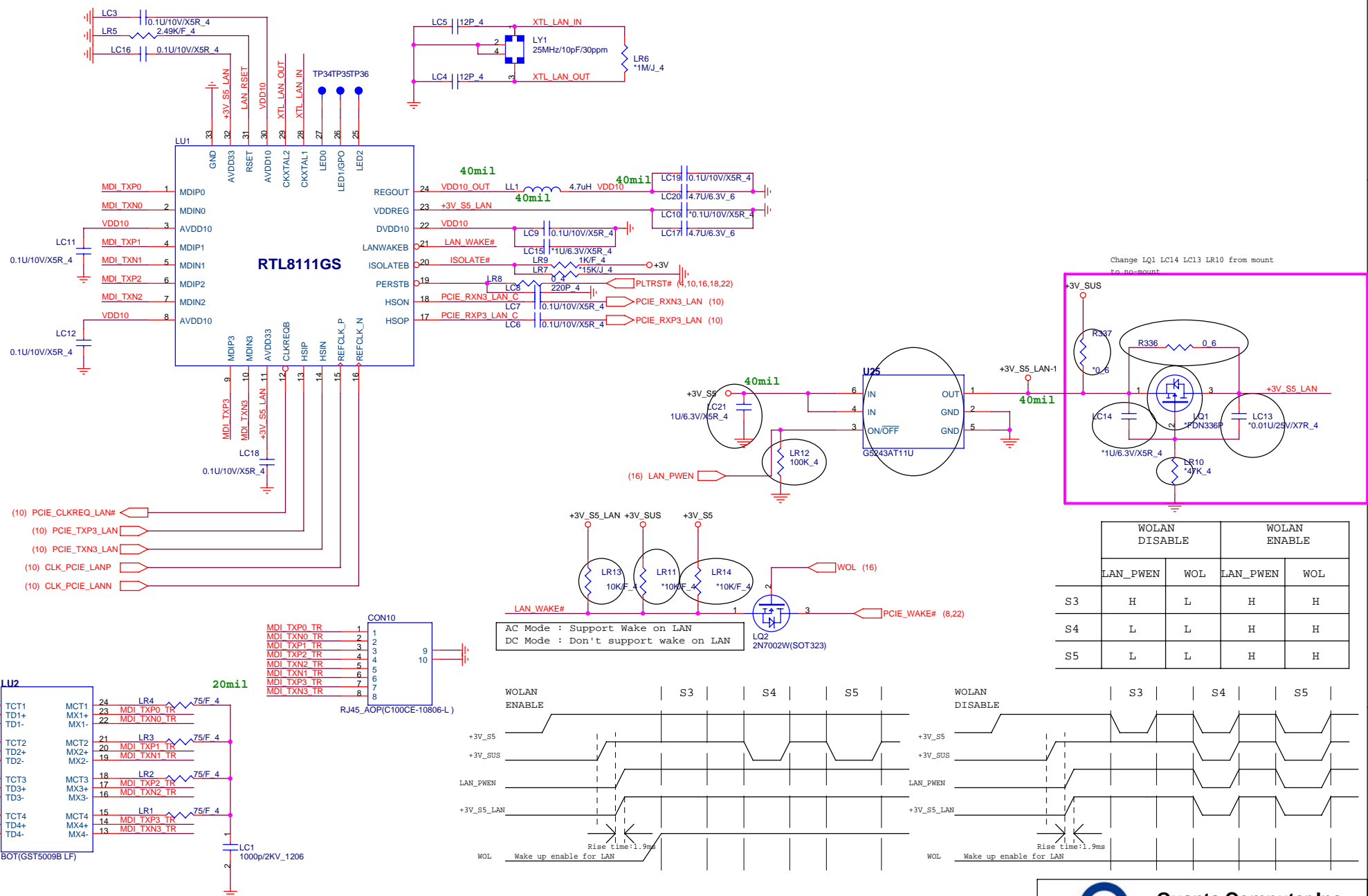
VBUS stop time 1Sec

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

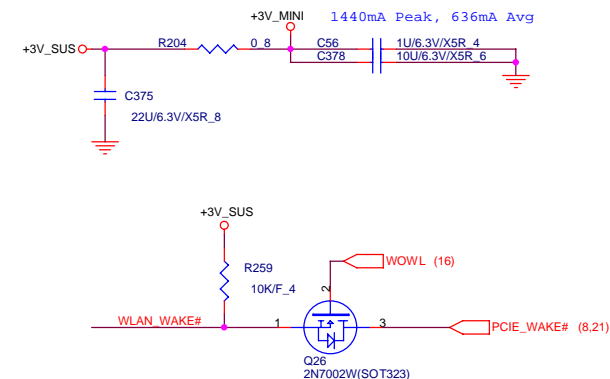
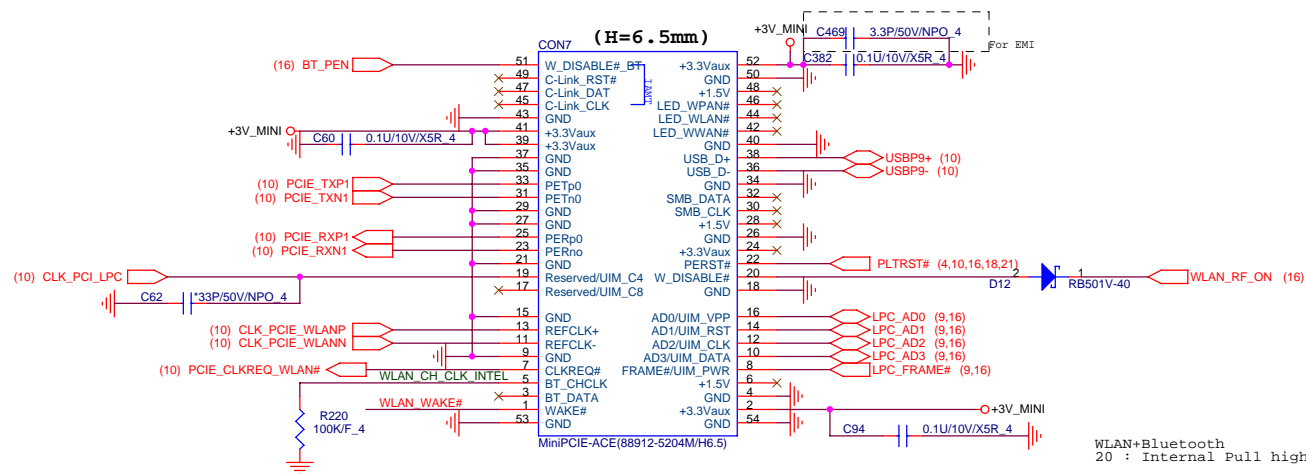
ILIM_SEL (I LIMIT(A)= 48000/R)		
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

 <b>Quanta Computer Inc.</b> <b>PROJECT :Chief River</b>		Rev 1A
Size	Document Number	
<b>USB/USB Charger</b>		
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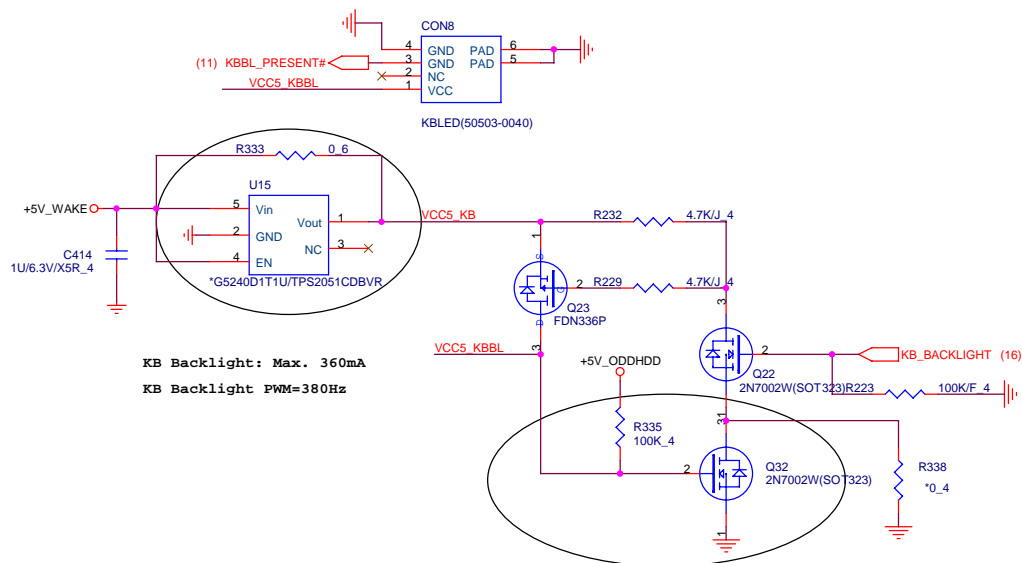


## WLAN/WIMAX/WIDI



AC Mode : Support Wake on WLAN  
DC Mode : Don't support wake on WLAN

## KB BACKLIGHT



Quanta Computer Inc.

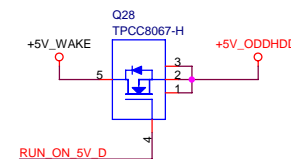
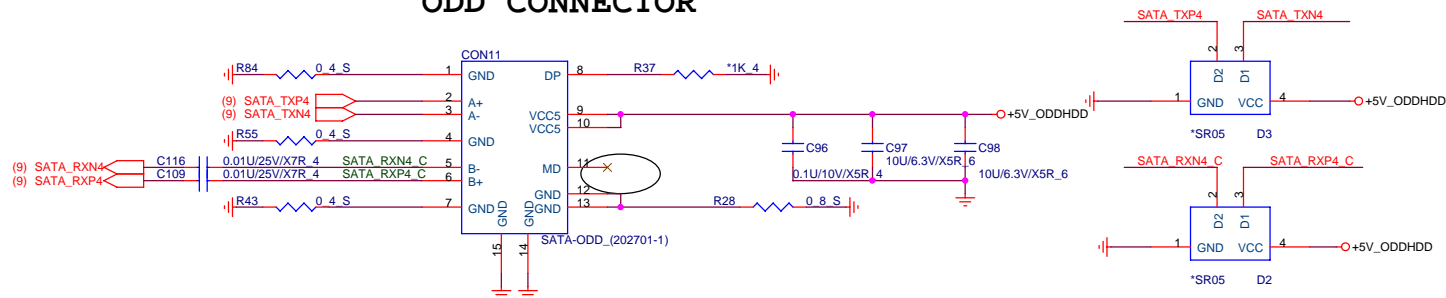
PROJECT :Chief River

WLAN/KB BL

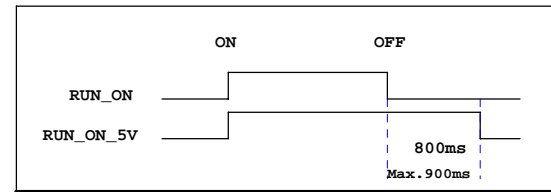
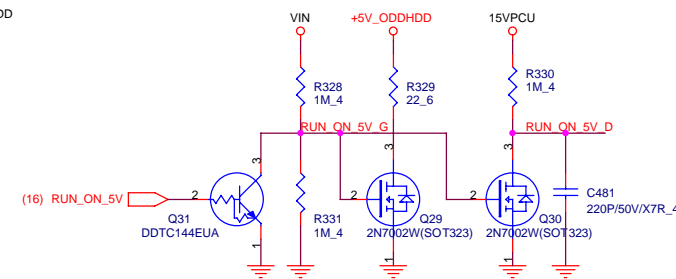
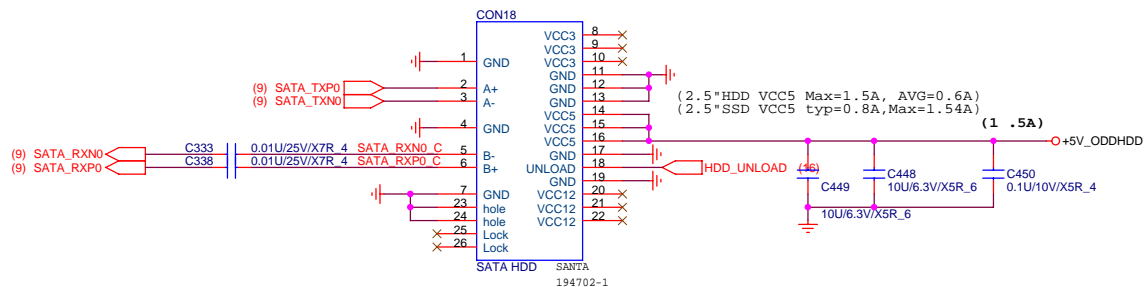
Size Document Number Rev 1A  
Date Thursday, January 17, 2013 Sheet 22 of 41

1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green Partners.

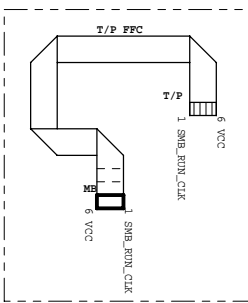
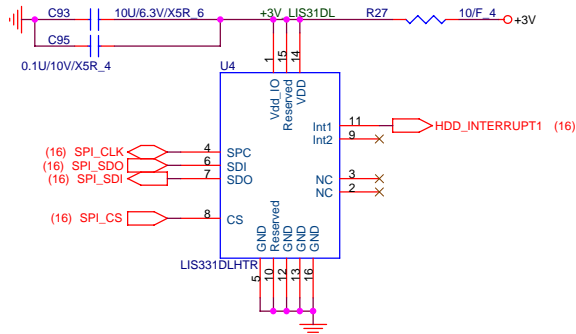
## ODD CONNECTOR



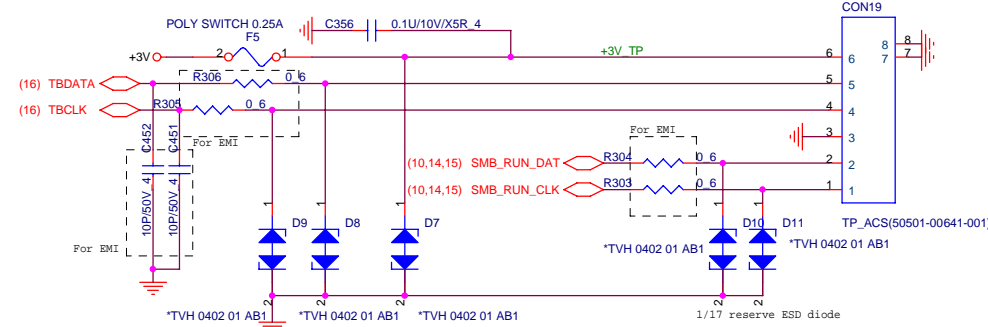
## HDD CONNECTOR



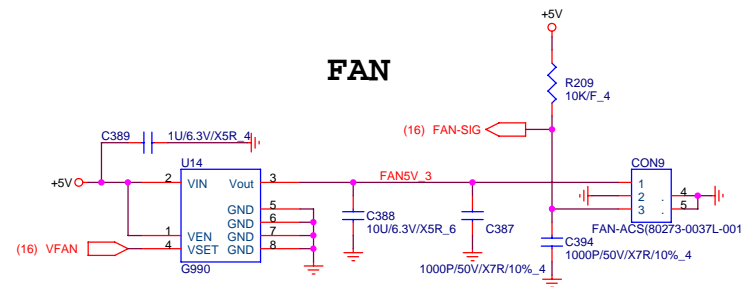
## HDD PROTECT SPI INTERFACE

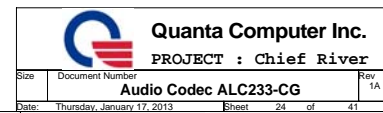
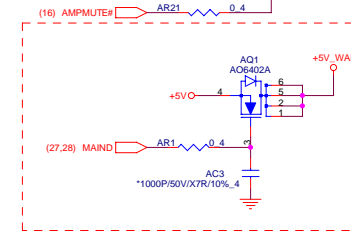


## T/P Board to T/P

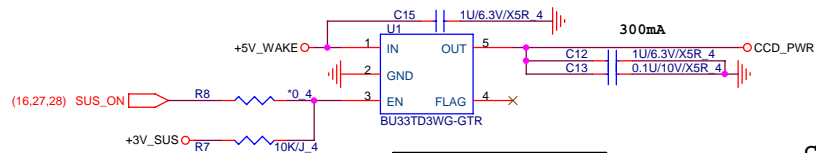


## FAN



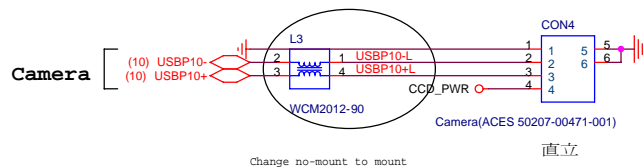


## USB Camera Power



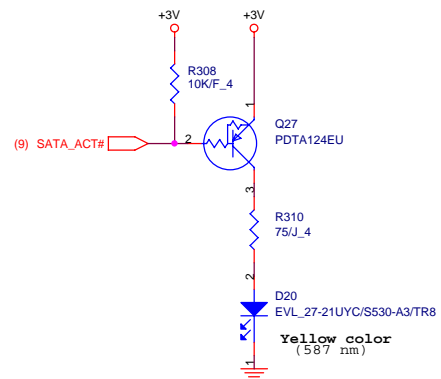
Camera HD specification  
Voltage: Max. 3.6V  
Current : Max. 200mA  
OCP: 200mA ~ 300mA

## Camera



## SATA LED

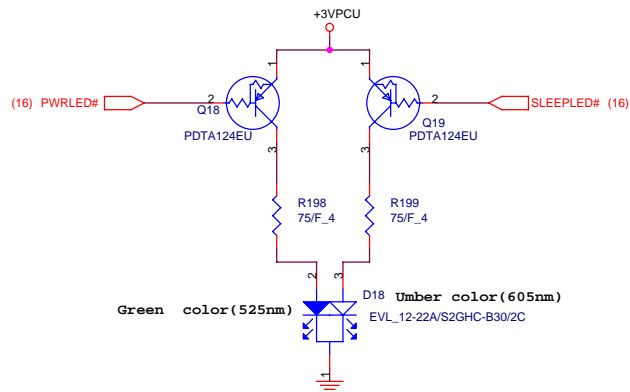
## BATTERY LED



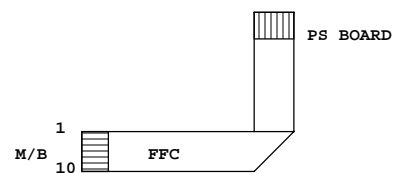
(16) BATLED1#

D19  
EVL\_27-21UYOC/S530-A3/TR8  
Umber Color

## Power/Sleep LED

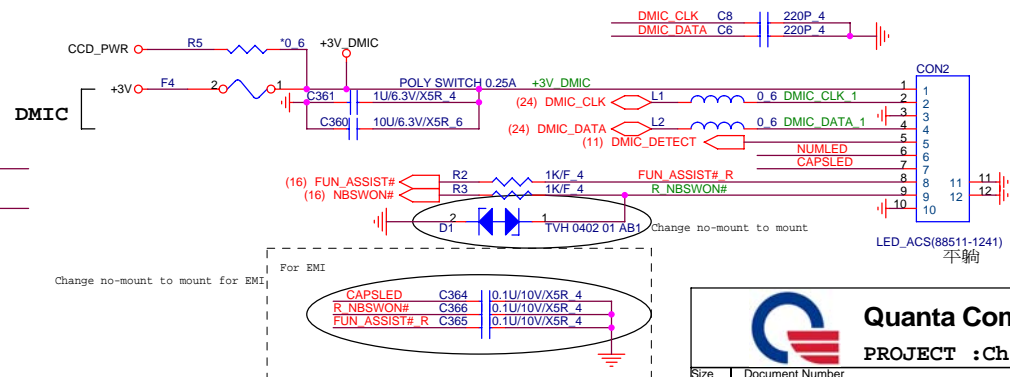


## Power SW Board Connector



(16) NUMLED# R1 150/F\_4 NUMLED

(16) CAPSLED# R4 150/F\_4 CAPSLED



1.Level 1 Environment-related Substances Should Never be Used.  
2.Recycled Resin and Coated Wire should be procured from Green  
Partners.



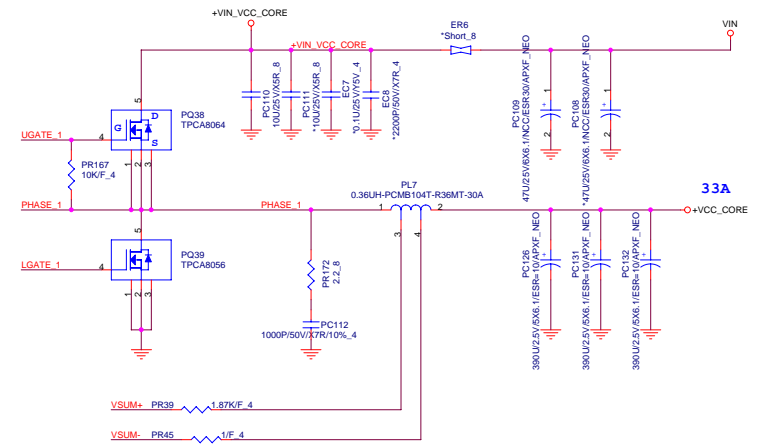
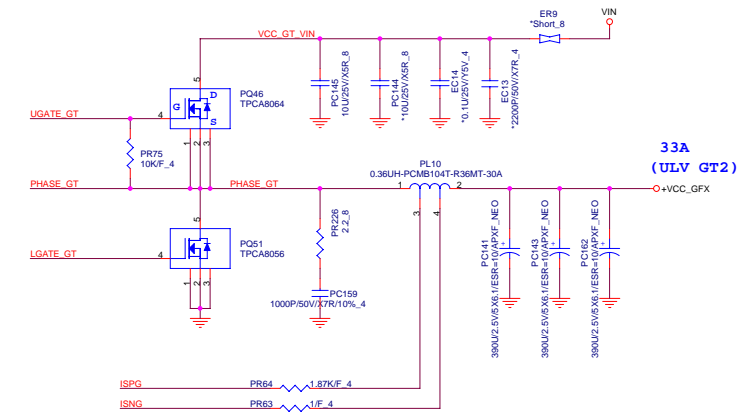
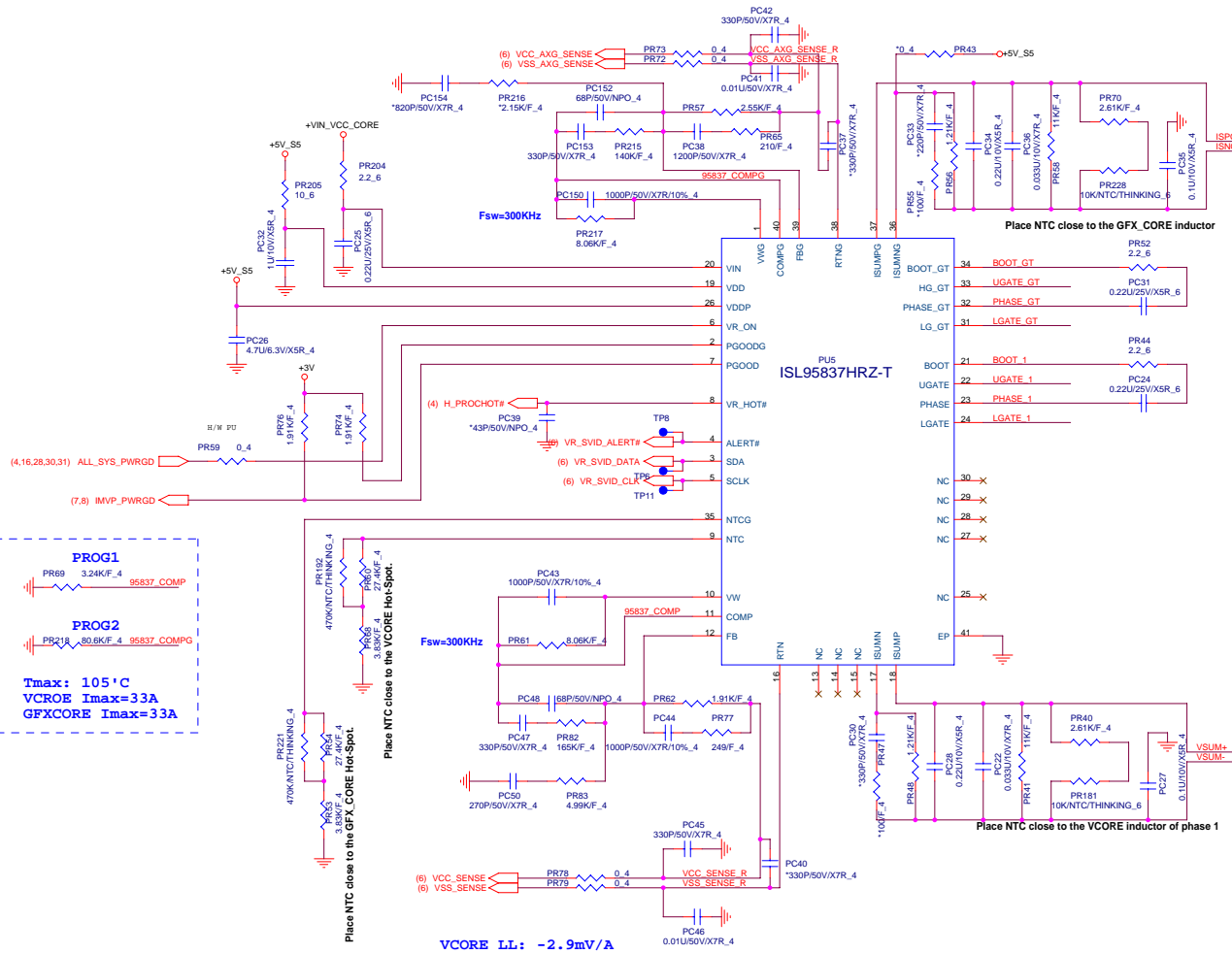
Quanta Computer Inc.

PROJECT :Chief River

LED/RF/KB/PS

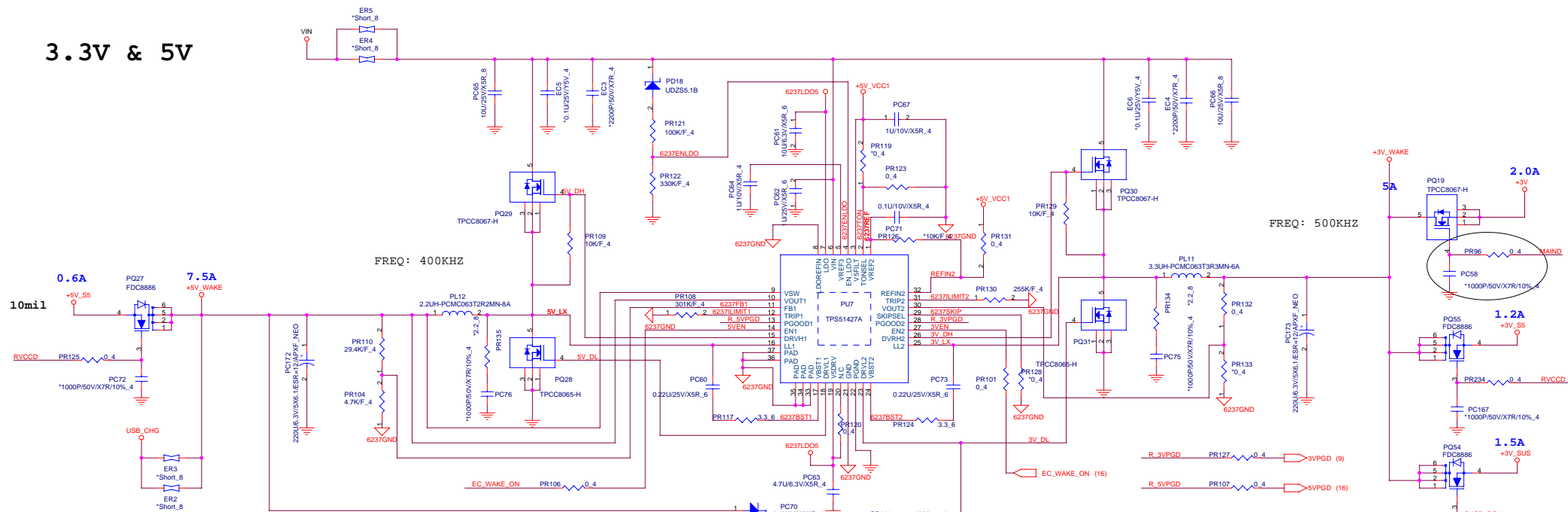
Size Document Number Rev 1A  
Date: Thursday, January 17, 2013 Sheet 25 of 41

GFX\_CORE LL: -3.9mV/A for GT2

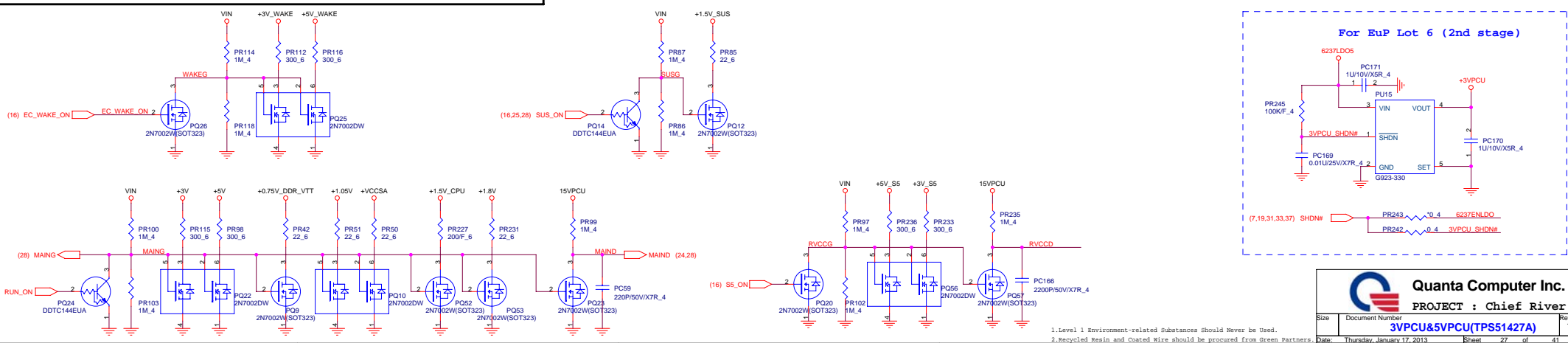
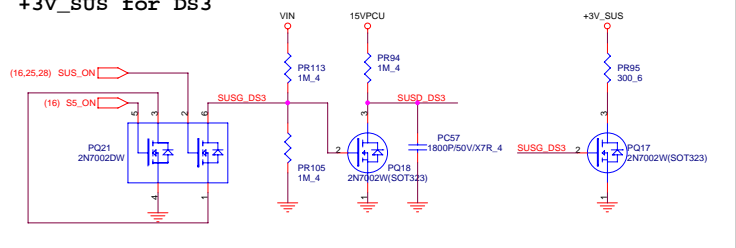




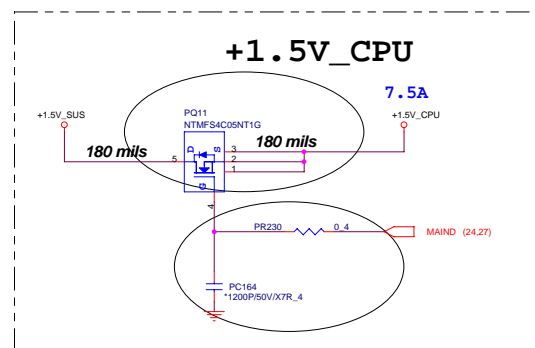
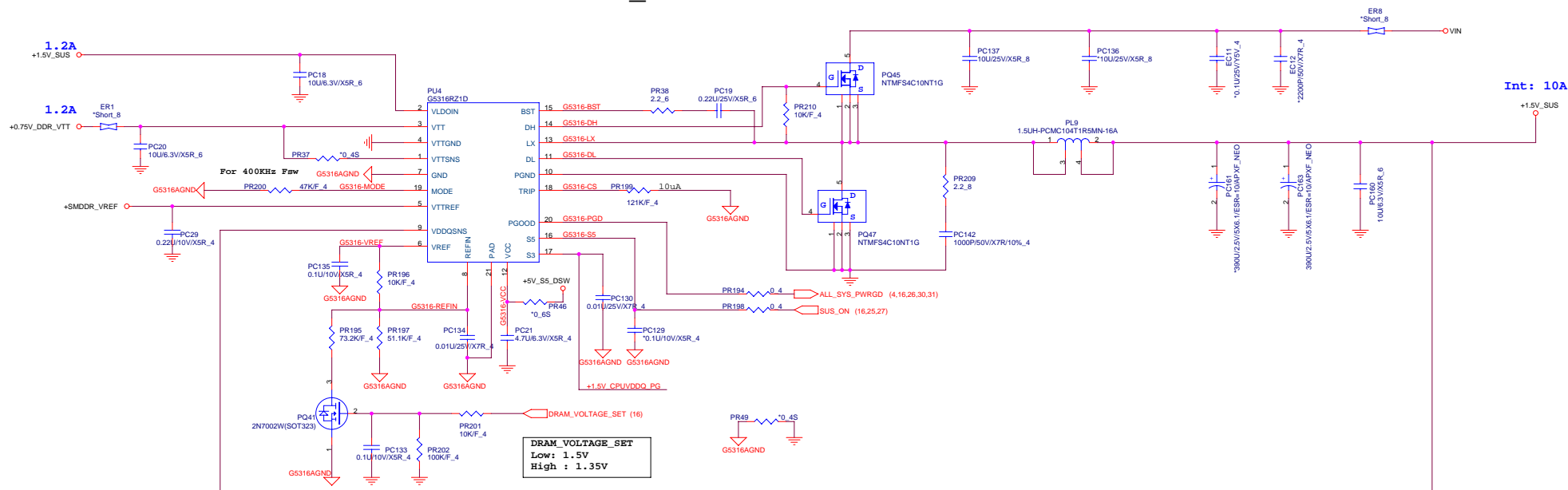
### 3.3V & 5V



## +3V\_SUS for DS3

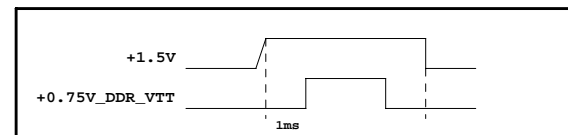
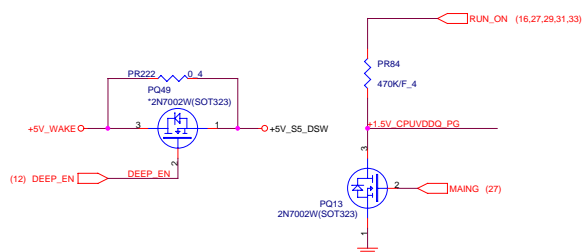


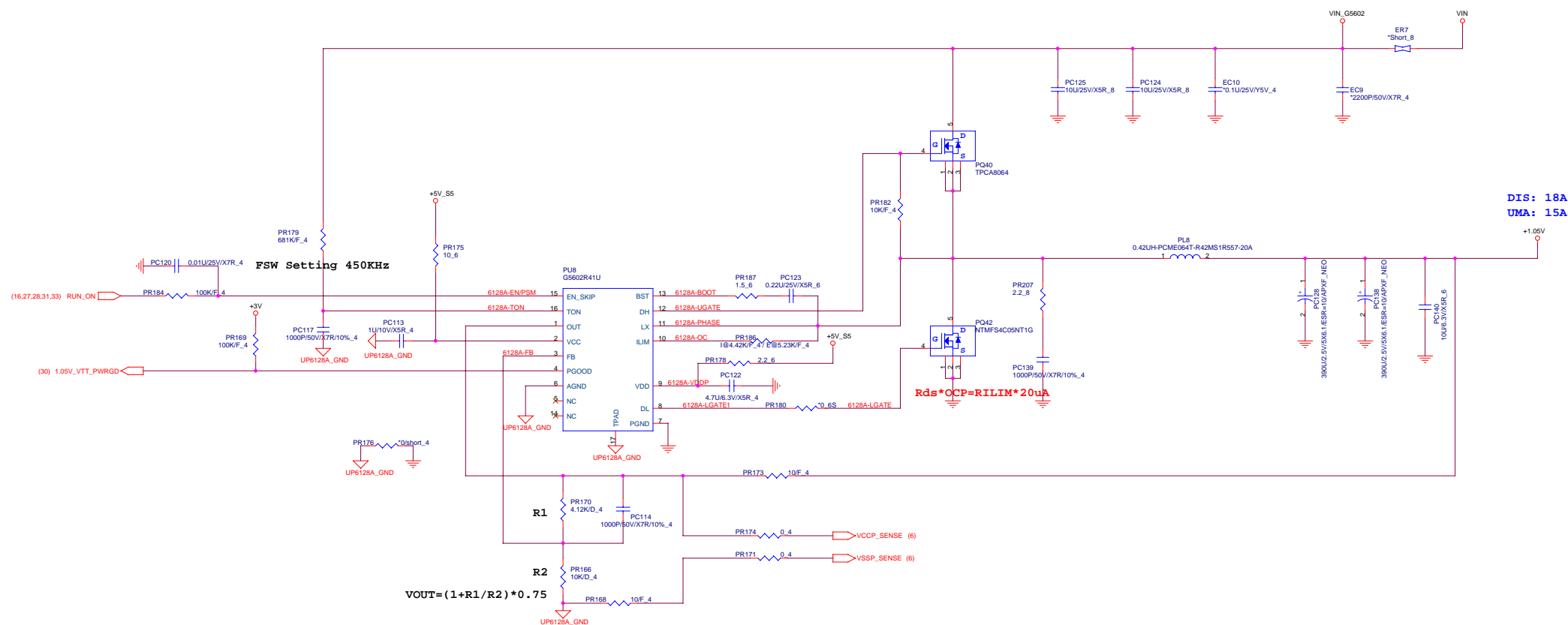
## 1.5VSUS & VTT\_MEM

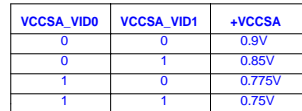


MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

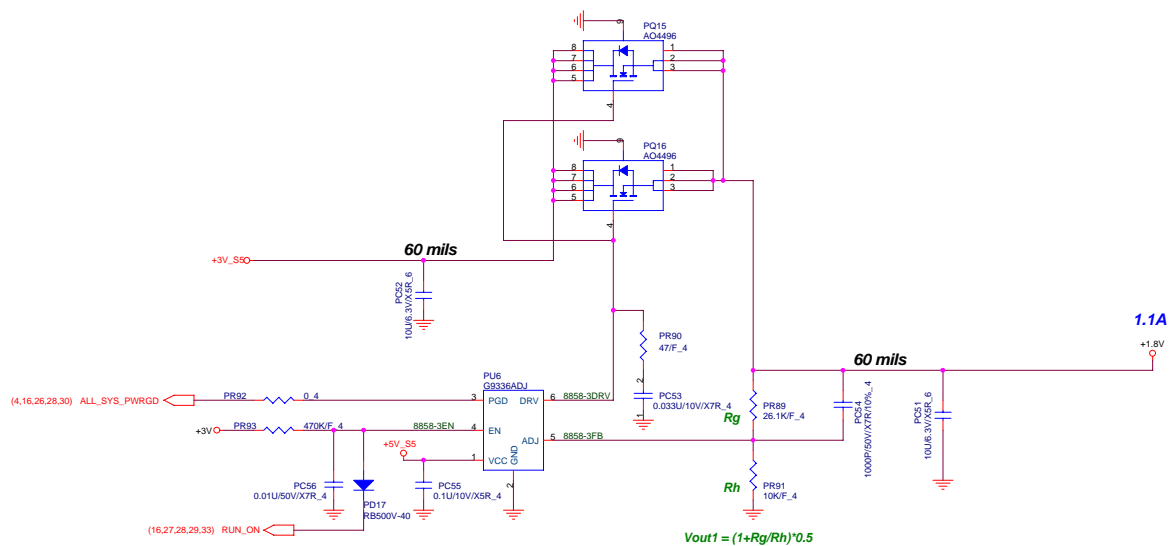
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



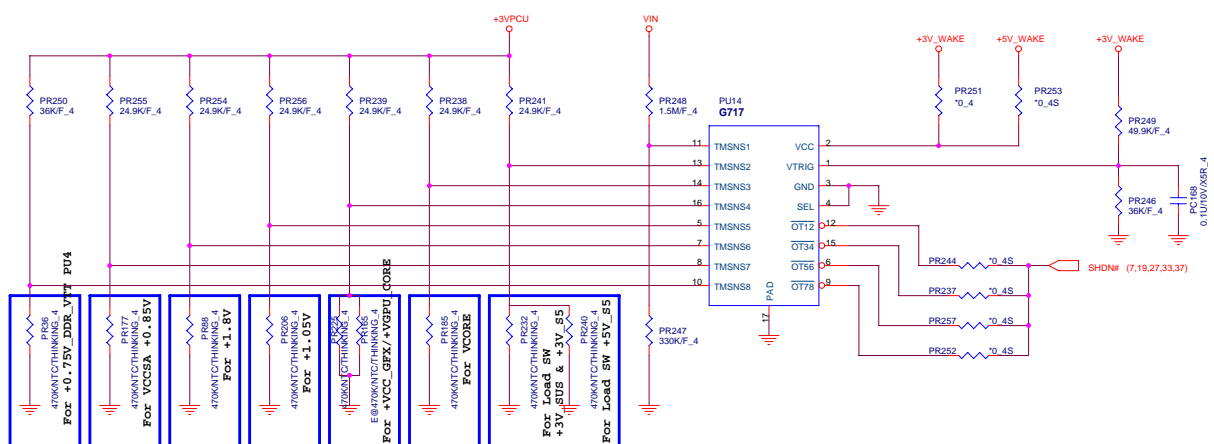


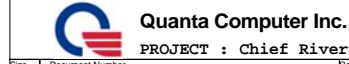


VCC1.8

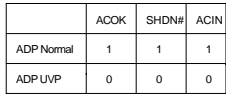


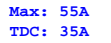
## Thermal Protection and Battery UVP for VEDS

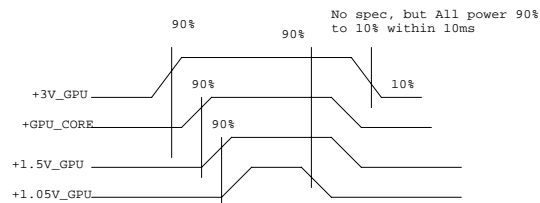
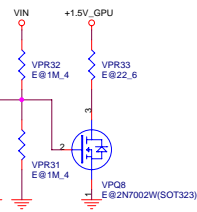
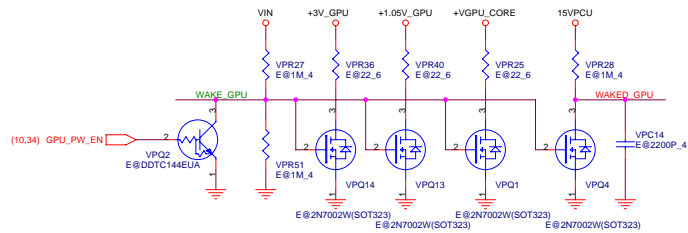
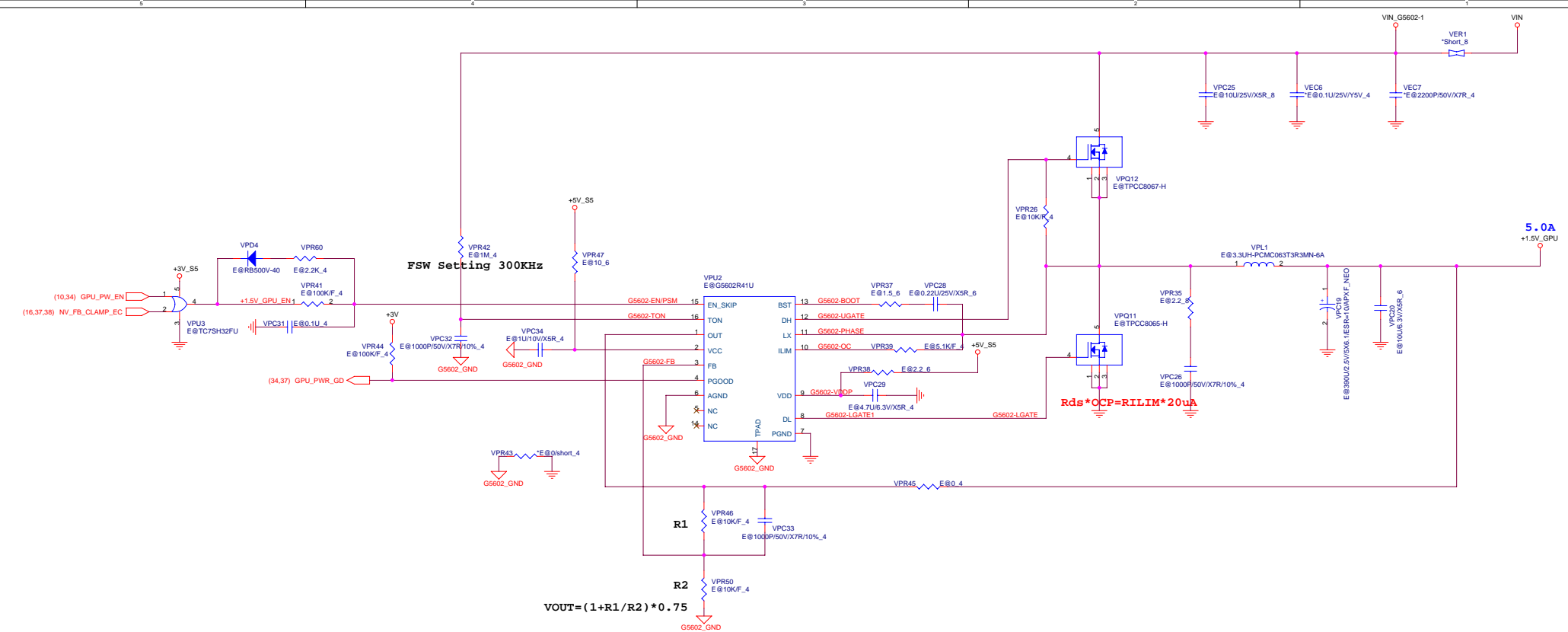






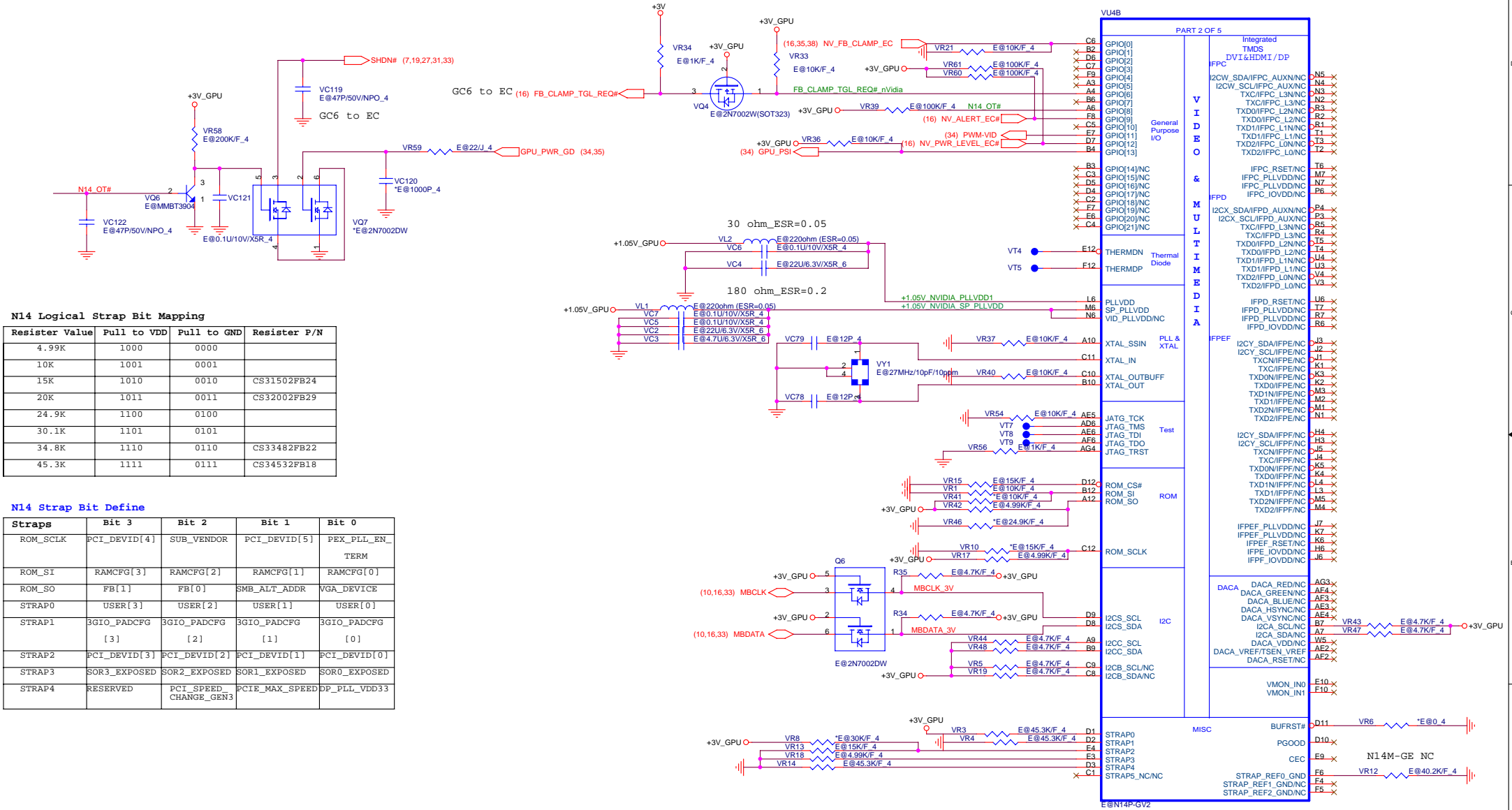








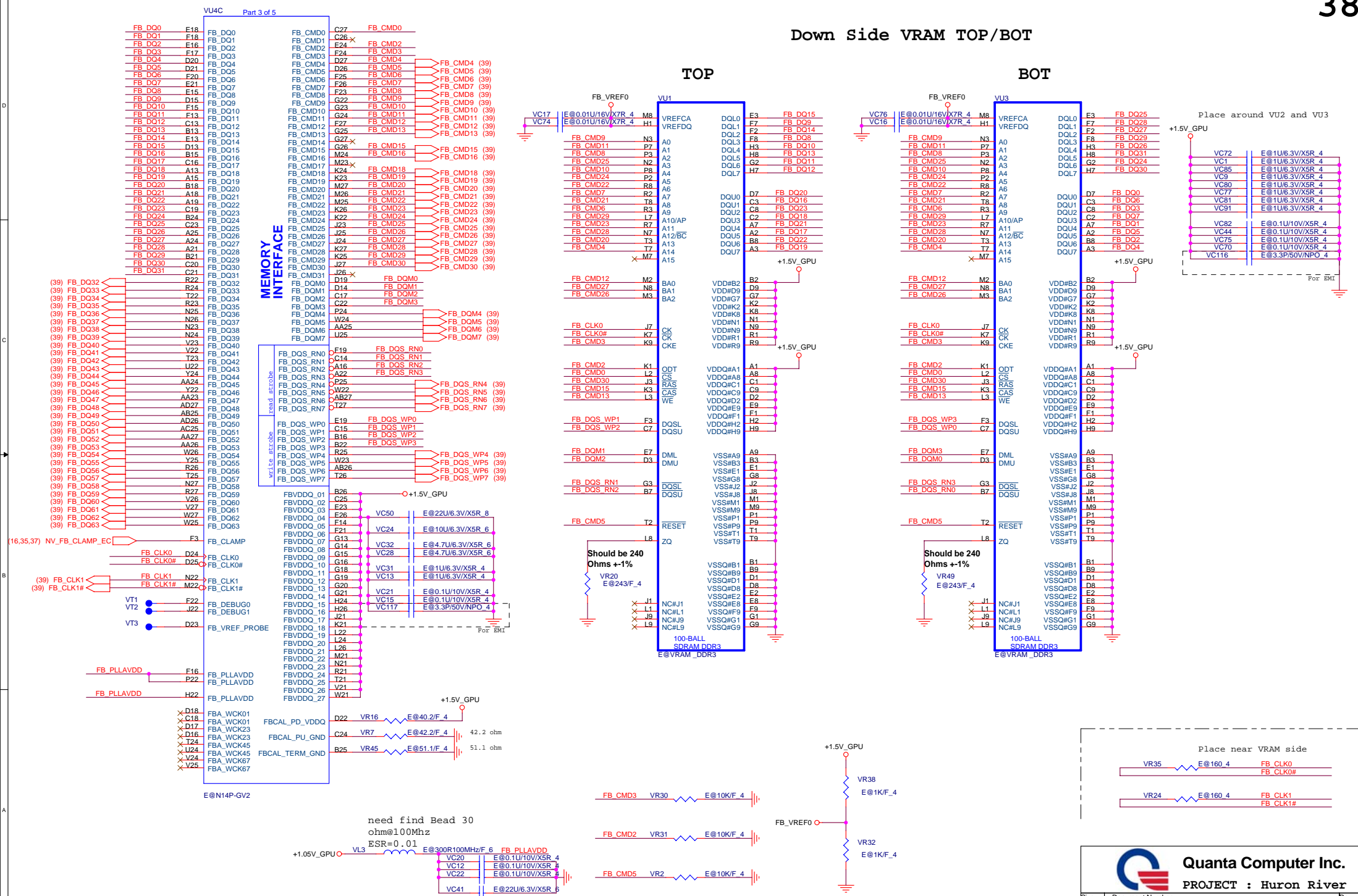
For GC6 GPU Monitor  
Status(FB\_CLAMP\_MON)



	VRAM Capacity	VRAM Vender	ID	VR1	Mfr P/N	Quanta P/N
N14M-LP N14P-GV2	128Mx16 DDR3	Samsung	0111	PD45.3K	K4W2G1646E-BC11	AKD5MGGT525
		Hynix	0110	PD34.8K	H5TQ2G63DPR-11C	AKD5MGWTW15
	256Mx16 DDR3	Samsung	0011	PD20K	K4W4G1646B-HC11	AKD5MGWT525
		Hynix	0010(TBD)	PD15K	H5TC4G63APR-11C	AKD5PGWTW10

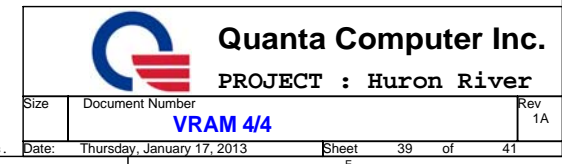
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## Down Side VRAM TOP/BOT



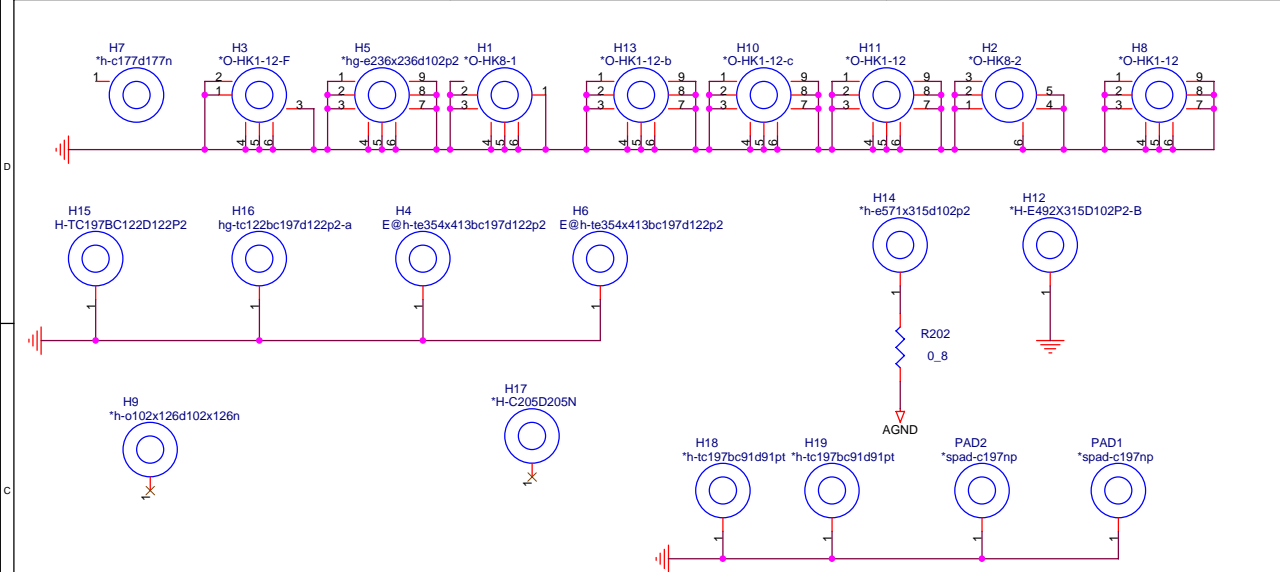


**BOT**

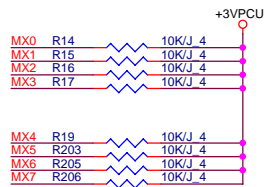
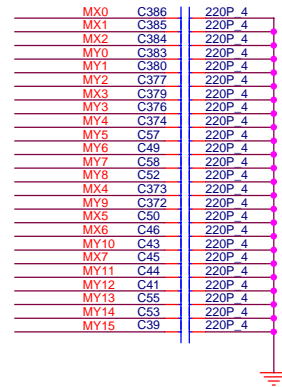
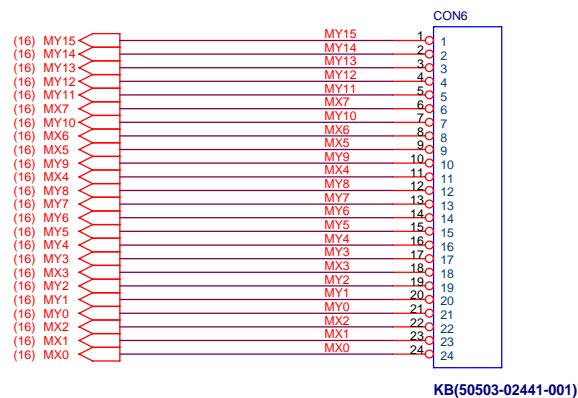


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2.Recycled Resin and Coated Wire should be procured from Green Partners.





## KEY BOARD Connector



USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN3.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	NFC
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	Card Reader
PORT 12	Touch Screen
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111G)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
Nvidia	1001 1110	-	1001 1110	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS35A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	0	1
Board ID0	CaspicCRA1-CaspicCRB1 HK8-HK9	SuperiorCRA1-SuperiorCRB1 GD5-GD6
Board ID1	HK8/GD5 14"	HK9/GD6 15"

PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff

	S0	S3	DS3	S4	S5 (Charger Enable)	S5 (Charger Disable)	S5 (Soft OFF) (WoL Disable)	S5 (Soft OFF) (WoL Enable)
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.8V	H	L	L	L	L	L	L	L
+1.8V_GPU	H	L	L	L	L	L	L	L
+1.0V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.5V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	H	L	L	H
+3V_WAKE	H	H	H	H	H	L	L	H
+5V_WAKE	H	H	H	H	H	L	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L